

Compal Confidential

QLA13/15 LA8501P Schematics Document

AMD Trinity APU with DDRIII + FCH Hudson D3

AIO M/B

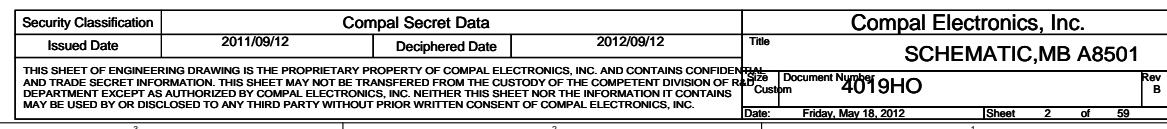
Friday, May 18, 2012

REV:1.0

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File Name : LA8501P

2 :HW TV



Voltage Rails

Power Plane	Description	S1	S3	S5
+12V1	Adapter power supply (12V)(For V_5V;V_3.3V;1.5V;12VS)	ON	ON	OFF
+12V2	Adapter power supply (12V)(For VGA_CORE;1.05VS;VRAM_1.5VS;CPU_CORE;VGFX_CORE)	ON	ON	OFF
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGFX_CORE	Graphics voltage for CPU	ON	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail for CPU	ON	OFF	OFF
+1.05VS_PCH	1.05V switched power rail for PCH	ON	OFF	OFF
+1.5V	1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail once PS_ON# low	ON	ON	OFF
+3VSB	3.3V power rail befor PS_ON# low	ON	ON	ON
+3.3V_LAN	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+V_3.3V	3.3V power rail once Adapter plug-in	ON	ON	OFF
+V_5V	5V power rail once Adapter plug-in	ON	ON	OFF
+5VSB	5V power rail befor PS_ON# low	ON	ON	ON
+5VALW	5V always on power rail once PS_ON# low	ON	ON	ON
+5VS	5V switched power rail	ON	OFF	OFF
+RTCVCC	RTC power	ON	ON	ON
+3VS_DGPU	3.3V power rail for GPU	ON	OFF	OFF
+VGA_CORE	Graphics power rail for GPU	ON	OFF	OFF
+1.05VS_DGPU	1.05VS switched power rail for GPU	ON	OFF	OFF
+VRAM_1.5VS	1.5VS power rail for VRAM	ON	OFF	OFF

EC SM Bus1 address

EC SM Bus2 address

Device	Address	HEX	Device	Address	HEX
ALC106	0100_100xb	48H	EMC1412-A (dGPU)	1111_100xb	F8H
			SB-TSI	1001-100xb	98H
			LVDS TR(RTD-2136S)	1001-010xb	0x94
			CPU CORE(IR3565MCP02TRP)		0x08

PCH SM Bus address

Device	Address
DDR DIMM1 (FCH_SMB0)	1001-000xb 90
DDR DIMM2 (FCH_SMB0)	1001-001xb 92
DDR DIMM3 (FCH_SMB0)	1001-010xb 94
DDR DIMM4 (FCH_SMB0)	1001-011xb 96

	Vendor	VRAM_ID0	VRAM_ID1	VRAM_ID2	
X7636838L04	Hynix 512	L	L	L	VRAM_ID0L@ VRAM_ID1L@ HYN512@
X7636838L02	Hynix 1G	H	L	L	VRAM_ID0H@ VRAM_ID1L@ HYN1G@
X7636838L03	Samsung 512	L	H	L	VRAM_ID0L@ VRAM_ID1H@ SAM512@
X7636838L01	Samsung 1G	H	H	L	VRAM_ID0H@ VRAM_ID1H@ SAM1G@

R1	SA000041S20	HYN512@	S IC D3 64MX16 H5TQ1G63DFR-11C
R3	SA000041S70		S IC D3 64M16 H5TQ1G63DFR-11C FBGA C38A!
R1	SA00004GS00	SAM512@	S IC D3 64M16 K4W1G1646G-BC11 FBGA 96P
R3	SA00004GS50		S IC D3 64M16 K4W1G1646G-BC11 FBGA C38A!
R1	SA00003YO00	HYN1G@	S IC D3 128MX16 H5TQ2G63BFR-11C FBGA 96P
R3	SA00003YO40		S IC D3 128M16 H5TQ2G63BFR-11C 96P C38A!
R1	SA00004Q000	SAM1G@	S IC D3 128M16 K4W2G1646C-HC11 FBGA 96P
R3	SA00004Q030		S IC D3 128M16 K4W2G1646C-HC11 96P C38A!

STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+VSB	+VS
Full ON		HIGH	HIGH	HIGH	ON	ON	ON
S1(Power On Suspend)		HIGH	HIGH	HIGH	ON	ON	ON
S3 (Suspend to RAM)		LOW	HIGH	HIGH	ON	ON	OFF
S4 (Suspend to Disk)		LOW	LOW	HIGH	ON	ON	OFF
S5 (Soft OFF)		LOW	LOW	LOW	OFF	ON	OFF

USB Port Table

USB 2.0	USB 1.1	Port	Device (D3 Only)
	OHCI	0	NC
		1	NC
EHCI1 DEV18 Fn2	OHCI	0	USB Conn B
		1	USB Conn B
		2	Touch Screen
		3	Camera
EHCI2 DEV19 Fn2	OHCI	4	USB Conn R
		5	MINI(WALN+BT)
		6	BT
		7	Mini Card(TV Tuner)
EHCI3 DEV22 Fn2	OHCI	8	HWTV
		9	USB Conn R
		10	
		11	
xHCI DEV16 Fn0 (D3 Only)	xHCI	12	USB30 Conn3
		13	USB30 Conn4
		0	
		1	
xHCI DEV16 Fn1	xHCI	2	USB 3.0 Port2
		3	USB 3.0 Port3

BOARD ID Table

Board ID	Ra/Rb	Vad-bid
AV SKU	R442 100K	3.3V
NON AV SKU	R445 0 ohm	0 V

BTO Option Table

BTO Item	BOM Structure
MBSC@	VGA@
HWTV@	UMA@
USB3@	DIS@
9012@	EC 9012@
DIS@	W/ DIS
930@	EC 930@
Hynix VRAM(512M)	HYN512@
Samsung VRAM(512M)	SAM512@
Hynix VRAM(1G)	HYN1G@
Samsung VRAM(1G)	SAM1G@

SKU ID(Project) Table

Project_ID2 (GPIO191)	Project_ID1 (GPIO190)	Project_ID0 (GPIO189)	SKU	BOM CONTROL @
0	0	0	UMA_w/o ATV	GPIO189L@ GPIO190L@ GPIO191L@ MBSC@ DAZ@
0	0	1	UMA_w/ ATV	GPIO189H@ GPIO190L@ GPIO191L@ HWTV@ DAZ@
0	1	0	DIS_512M_w/o ATV	GPIO189L@ GPIO190H@ GPIO191L@ MBSC@ DIS@ DAZ@ X7636838L04
0	1	1	DIS_512M_w/ ATV	GPIO189H@ GPIO190H@ GPIO191L@ HWTV@ DIS@ DAZ@ X7636838L04
1	0	0	DIS_1G_w/o ATV	GPIO189L@ GPIO190L@ GPIO191H@ MBSC@ DIS@ DAZ@ X7636838L02
1	0	1	DIS_1G_w/ ATV	GPIO189H@ GPIO190L@ GPIO191H@ HWTV@ DIS@ DAZ@ X7636838L02
1	1	0	X	
1	1	1	X	

VRAM_ID0L@	R1233	SD028100280
VRAM_ID1L@	R1234	SD028100280
VRAM_ID0H@	R1230	SD028100280
VRAM_ID1H@	R1231	SD028100280

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D

C

B

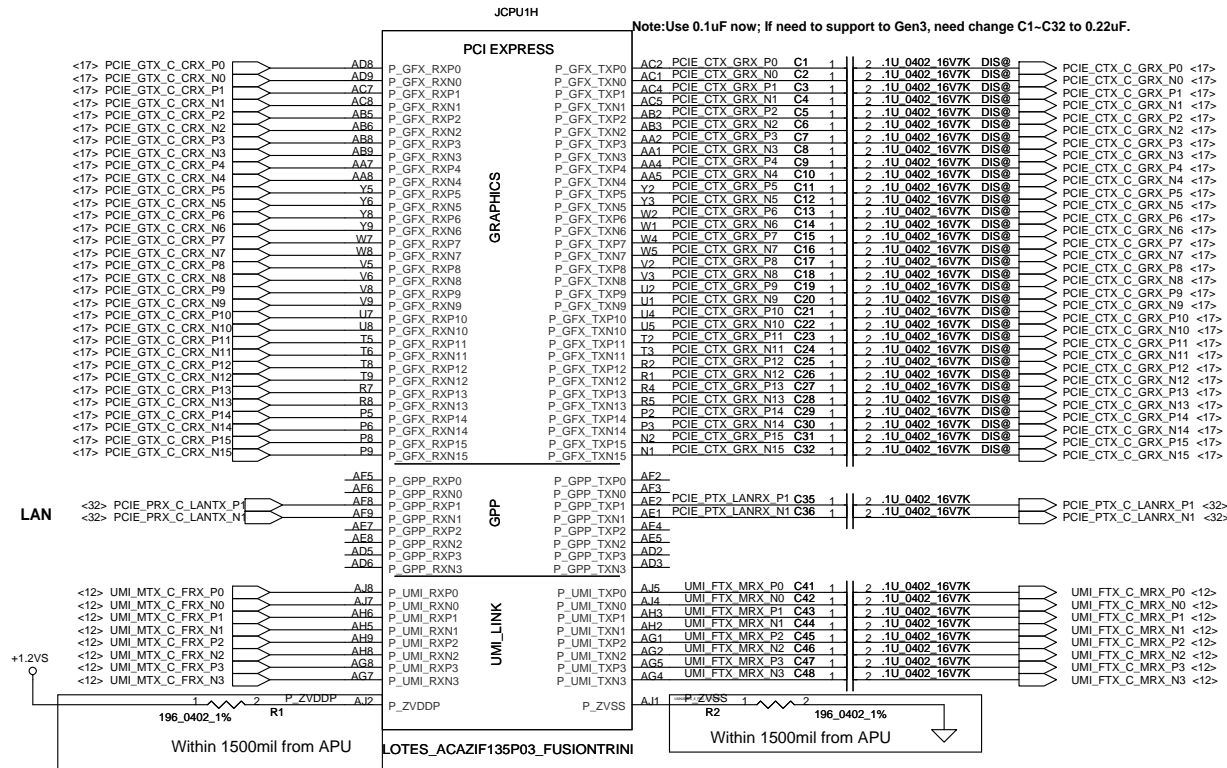
A

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A



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<10> DDR_A_DQS[0..7]
<10> DDR_A_DQS#[0..7]

<10> DDR_A_D[0..63]

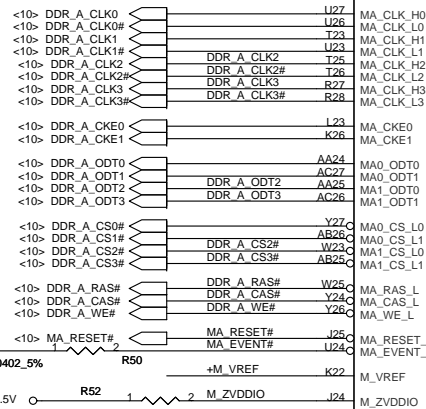
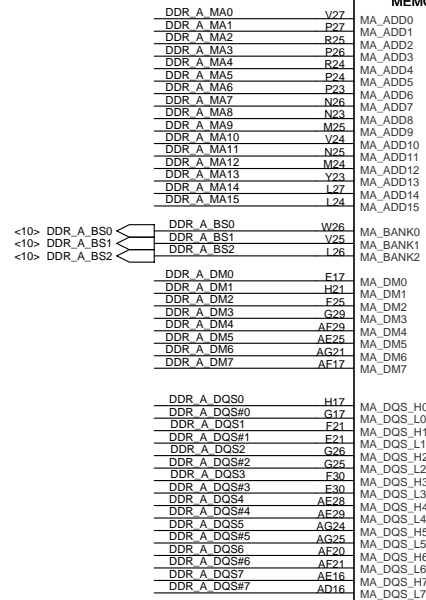
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<11> DDR_B_D[0..63]

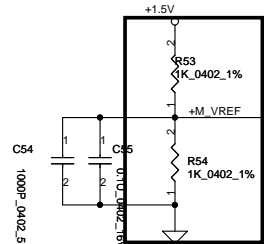
JCPU1A

MEMORY CHANNEL A

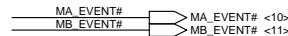


1116 modify

PLACE WITHIN 1.5" OF APU

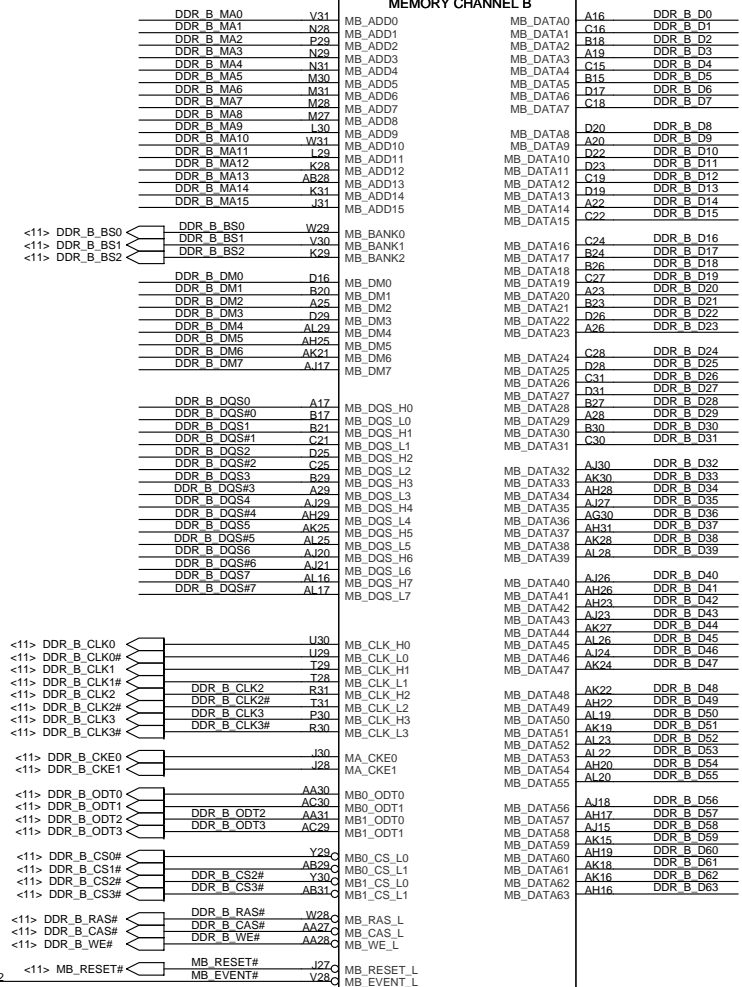


LOTES_ACAZIF135P03_FUSIONTRINI



JCPU1B

MEMORY CHANNEL B

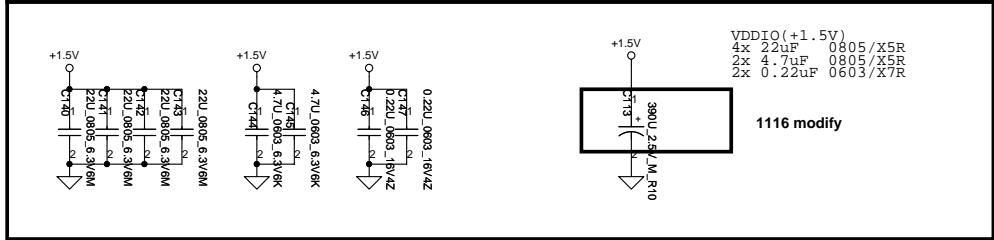


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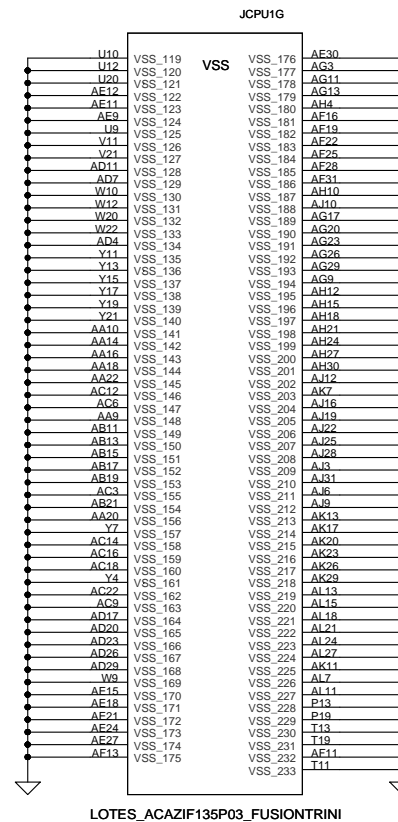
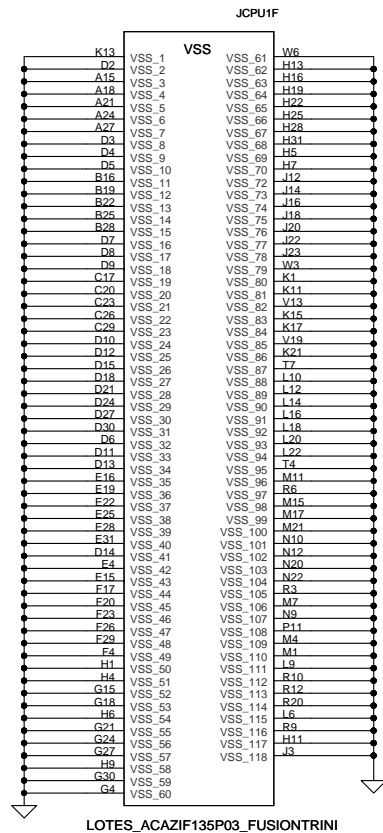
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+CPU_CORE At PWR Page53

+CPU_CORE_NB At PWR Page53



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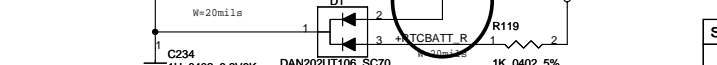
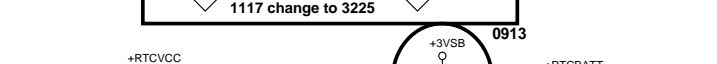
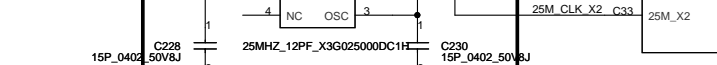
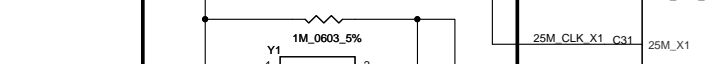
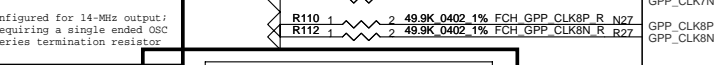
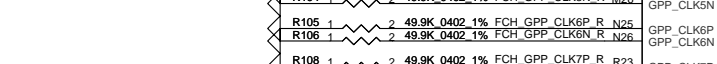
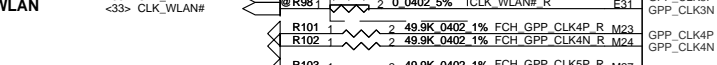
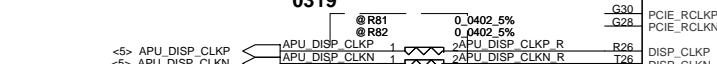
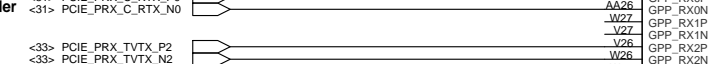
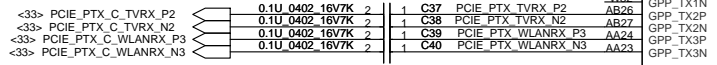
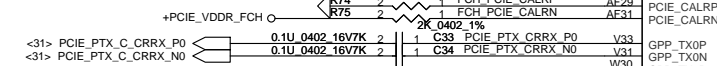
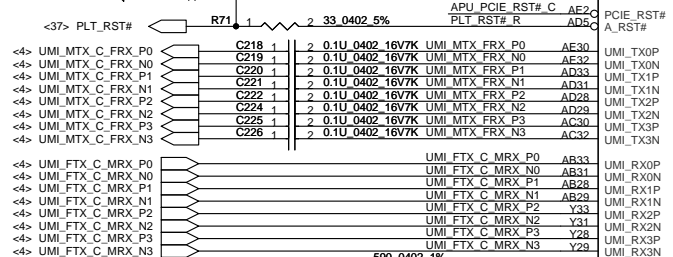
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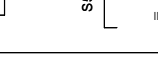
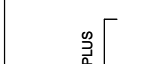
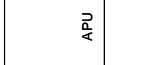
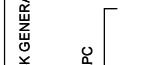
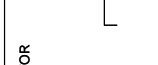
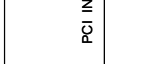
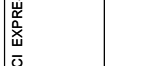
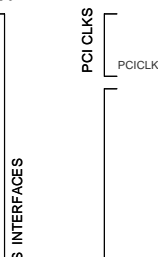


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PCI Host Bus Reset (To EC) C217 1 2 150P_0402_50V8J

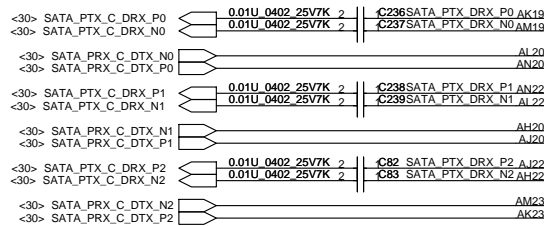


HUDSON-2

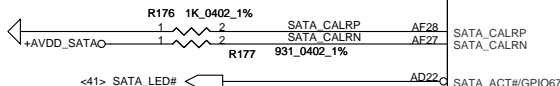


HDD

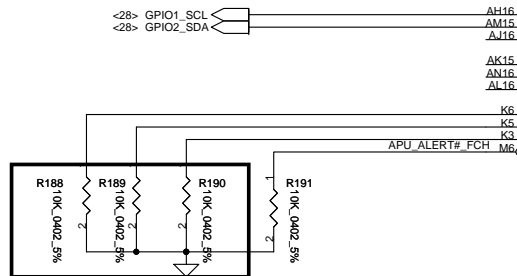
ODD



PUT SATA_CAL Resistors close to U600



Integrated Clock Mode: Left unconnected



U1B

HUDSON-2

Part 2 of 5

SD CARD

GBE LAN

SPI ROM

SERIAL ATA

VGA DAC

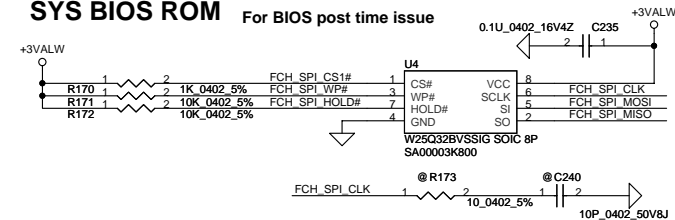
VGA MAINLINK

HW MONITOR

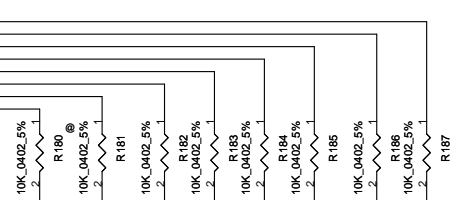
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SYS BIOS ROM

For BIOS post time issue



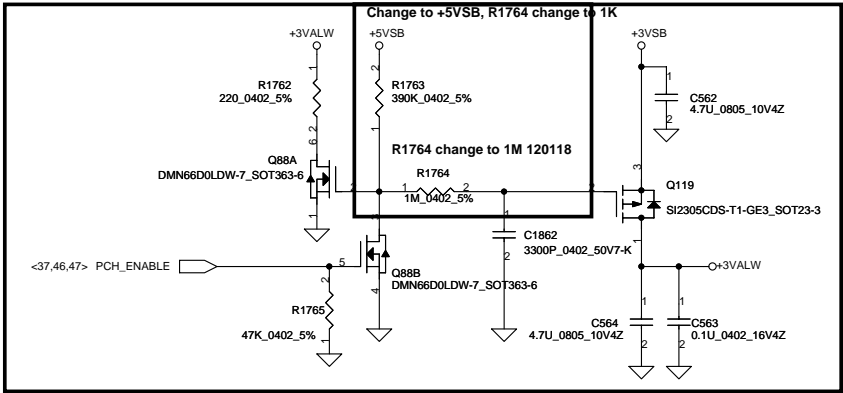
0319



Use as GPIO or configure for one of the following options if not used.

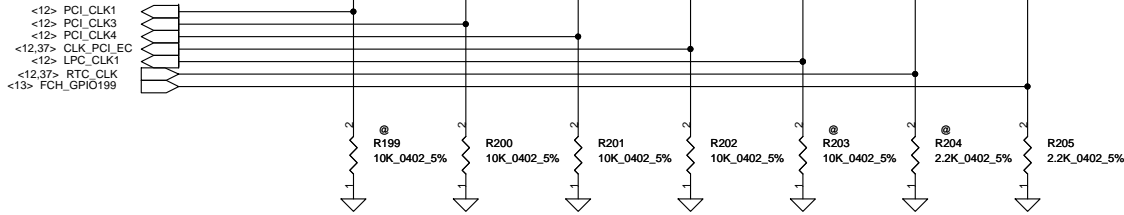
- 10-KΩ 5% pull-up resistor to +3.3V_S5.
- 10-KΩ 5% pull-down resistor.

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STRAP PINS

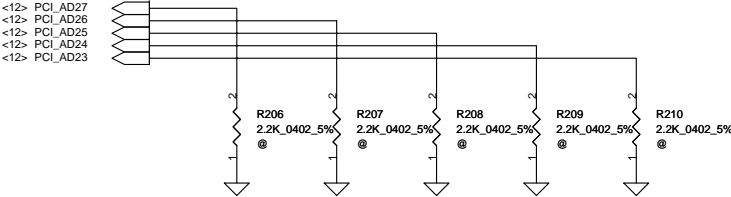
	PCI_CLK1	PCI_CLK3	PCI_CLK4	CLK_PCI_EC	LPC_CLK1	FCH_GPIO199	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED



DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	RESERVED	Normal REFCLK termination DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	RESERVED	Inverted REFCLK termination	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

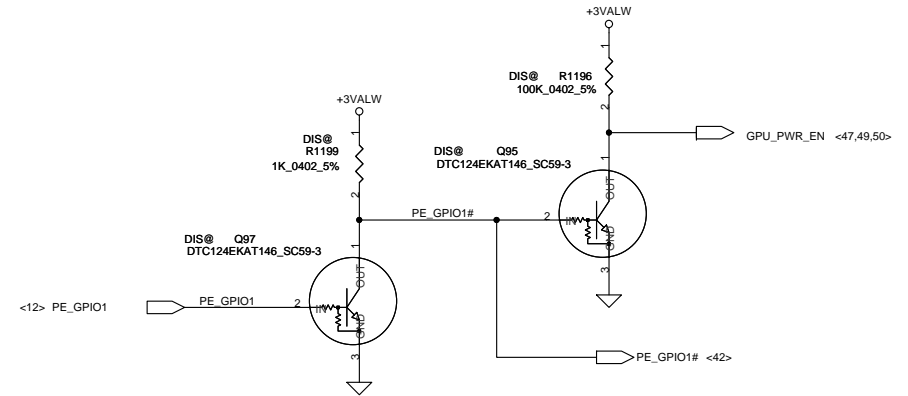
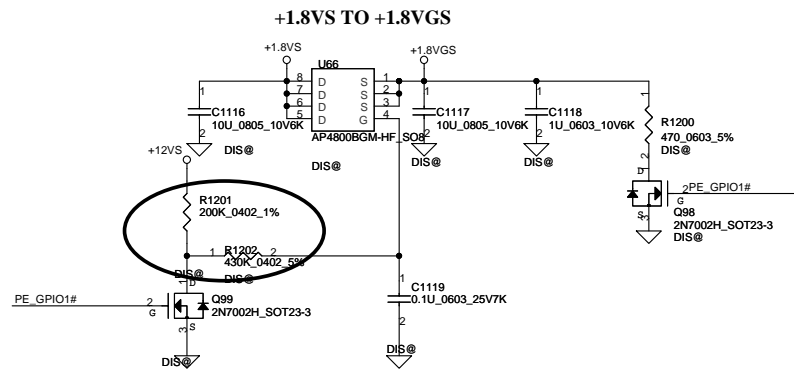
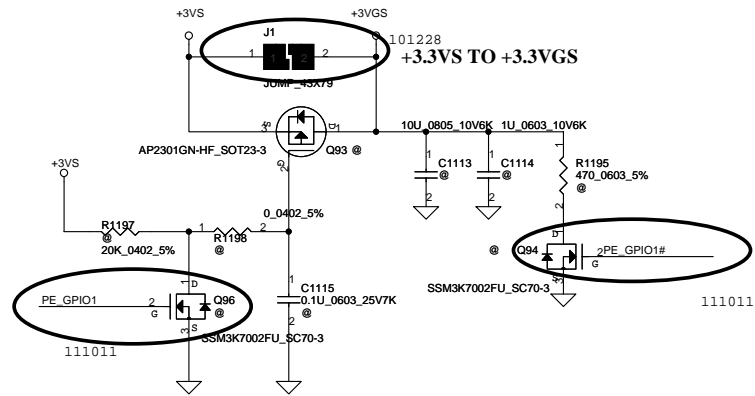


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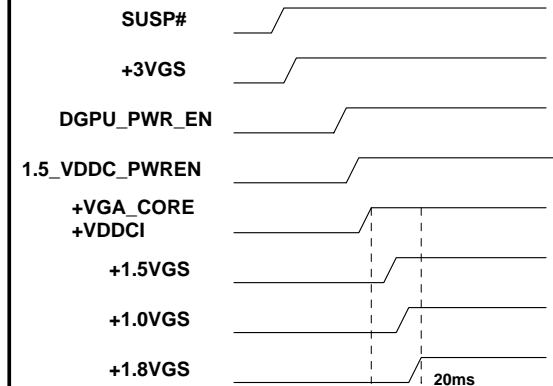
2180755011A14 HUDSON_FCBGA656

For FCH
D2 - BOM option
VDDAN_11_SSUSB_S / VDDCR_11_SSUSB_S/VDDPL_33_SSUSB_S
Connected to VSS.
D3-VDDAN_11_SSUSB_S / VDDCR_11_SSUSB_S
Connected to +1.1ALW &
VDDPL_33_SSUSB_S connect to +3.3ALW

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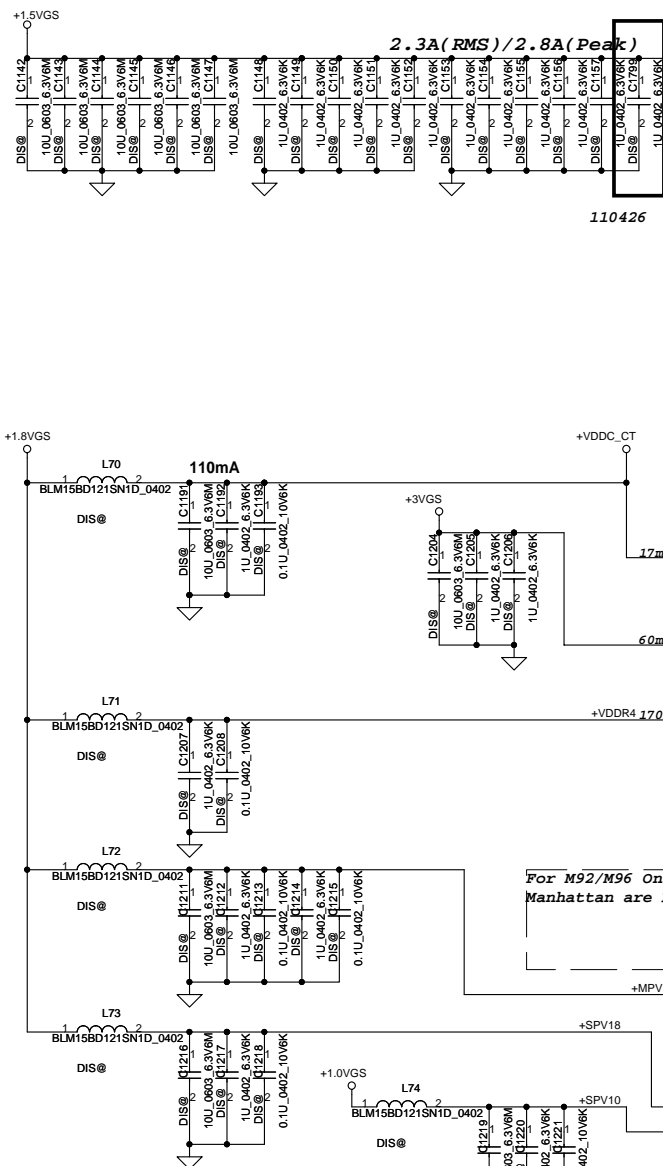
Power Sequence of Whistler and Seymour



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For M92/M96 Only
Manhattan are NC pin

Source	dist.	0.1u	1u	10u
1.5VGS	VDDR1	10	10	5
1.8VGS	PCIE_VDDR	2	3	1
VGA_core	PCIE_VDDC	7	1	
	VDDC	25	6	

2.3A(RMS)/2.8A(Peak)

110426

AC7
AD11
AF7
AG10
A17
AK8
VDDR1#15
VDDR1#16
VDDR1#17
VDDR1#18
VDDR1#19
G11
G14
G17
G20
G23
G26
G29
H10
VDDR1#15
VDDR1#16
VDDR1#17
VDDR1#18
VDDR1#19
K8
VDDR1#20
VDDR1#21
L16
L21
L23
L26
L7
M11
N11
P7
R11
U11
U7
Y11
Y7

LEVEL
TRANSLATION

VDD_CT#1
VDD_CT#2
VDD_CT#3
VDD_CT#4

I/O

VDDR3#1
VDDR3#2
VDDR3#3
VDDR3#4

VDDR4#4
VDDR4#5
VDDR4#7
VDDR4#8
VDDR4#1
VDDR4#2
VDDR4#3
VDDR4#6

NC_VDDRHA
NC_VSSRHA
NC_VDDRHB
NC_VSSRHB

PLL

MPV18#1
MPV18#2

VOLTAGE
SENSE

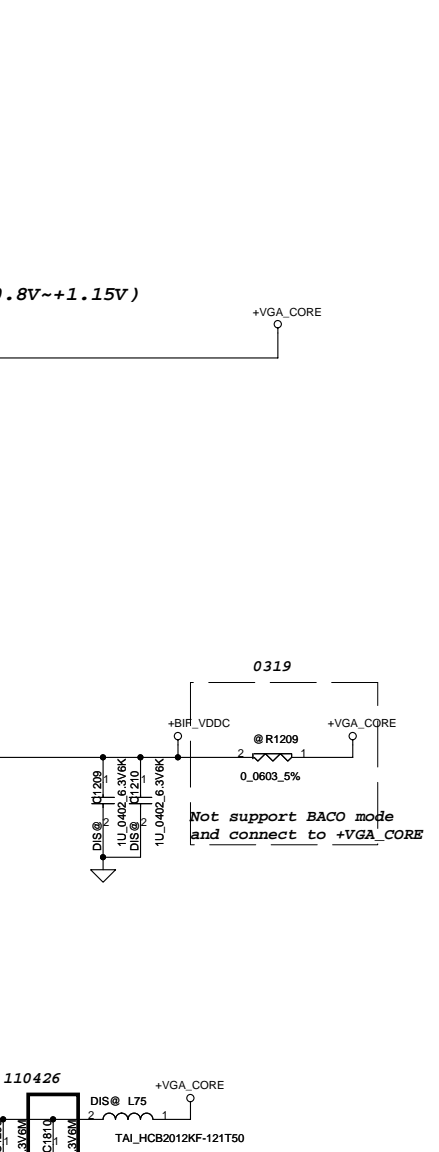
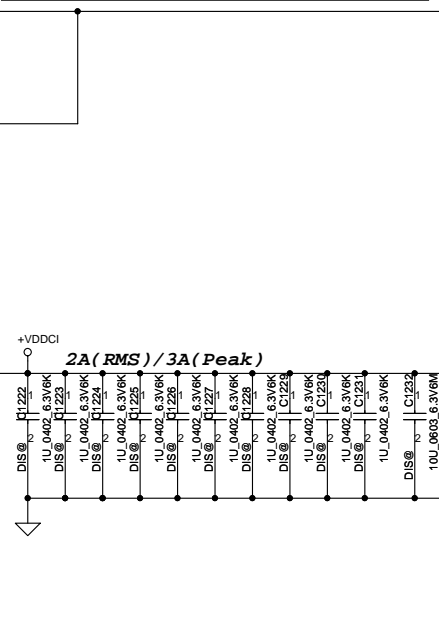
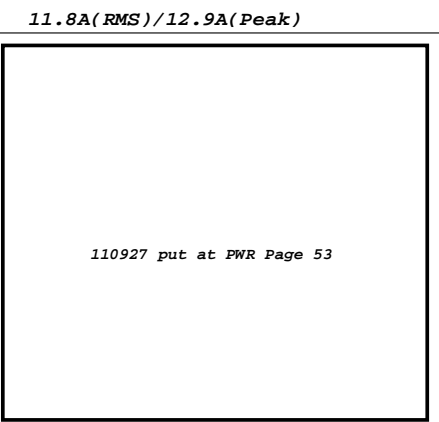
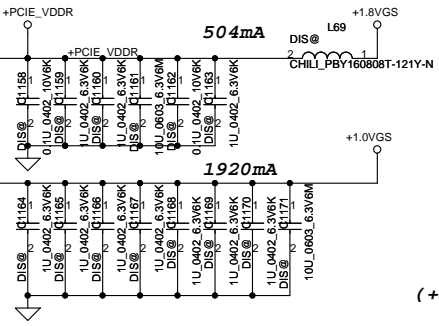
FB_VDDC
FB_VDDCI
FB_GND

VDDR1#1
VDDR1#2
VDDR1#3
VDDR1#4
VDDR1#5
VDDR1#6
VDDR1#7
VDDR1#8
VDDR1#9
VDDR1#10
VDDR1#11
VDDR1#12
VDDR1#13
VDDR1#14
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VDDR1#18
VDDR1#19
VDDR1#20
VDDR1#21
VDDR1#22

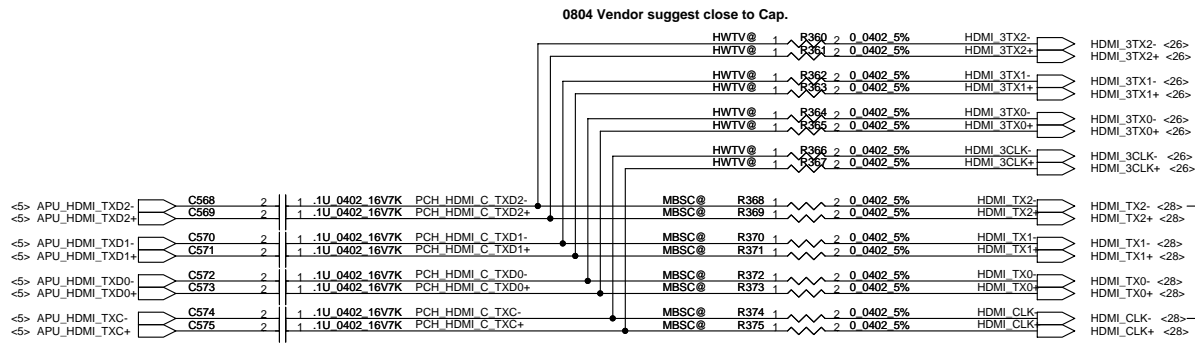
PCIE_VDDR#1
PCIE_VDDR#2
PCIE_VDDR#3
PCIE_VDDR#4
PCIE_VDDR#5
PCIE_VDDR#6
PCIE_VDDR#7
PCIE_VDDR#8
PCIE_VDDR#9
PCIE_VDDC#1
PCIE_VDDC#2
PCIE_VDDC#3
PCIE_VDDC#4
PCIE_VDDC#5
PCIE_VDDC#6
PCIE_VDDC#7
PCIE_VDDC#8
PCIE_VDDC#9
PCIE_VDDC#10
PCIE_VDDC#11
PCIE_VDDC#12

VDDC#1
VDDC#2
VDDC#3
VDDC#4
VDDC#5
VDDC#6
VDDC#7
VDDC#8
VDDC#9
VDDC#10
VDDC#11
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VDDC#47
VDDC#48
VDDC#49
VDDC#50
VDDC#51
VDDC#52
VDDC#53
VDDC#54
VDDC#55
VDDC#56
VDDC#57
VDDC#58

VDDCI#1
VDDCI#2
VDDCI#3
VDDCI#4
VDDCI#5
VDDCI#6
VDDCI#7
VDDCI#8
VDDCI#9
VDDCI#10
VDDCI#11
VDDCI#12
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VDDCI#21
VDDCI#22

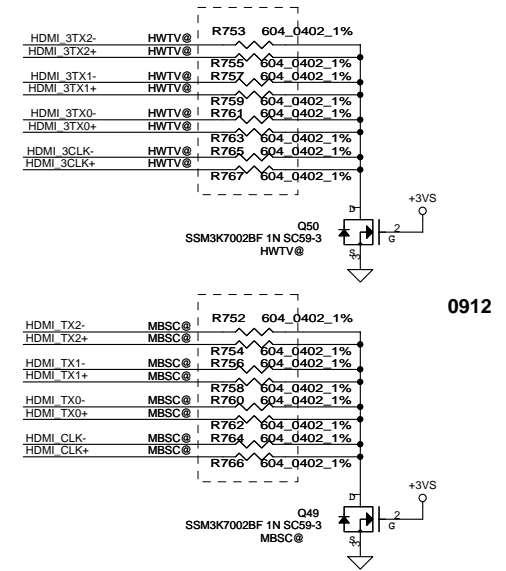




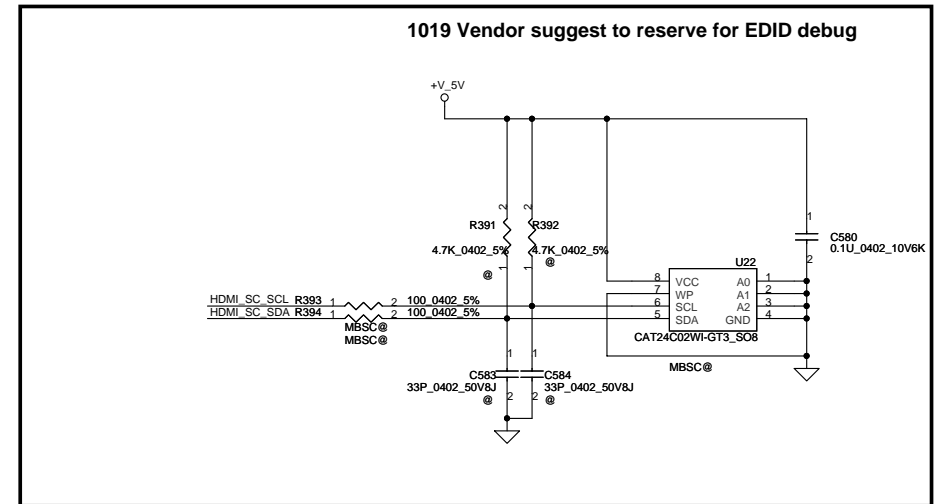
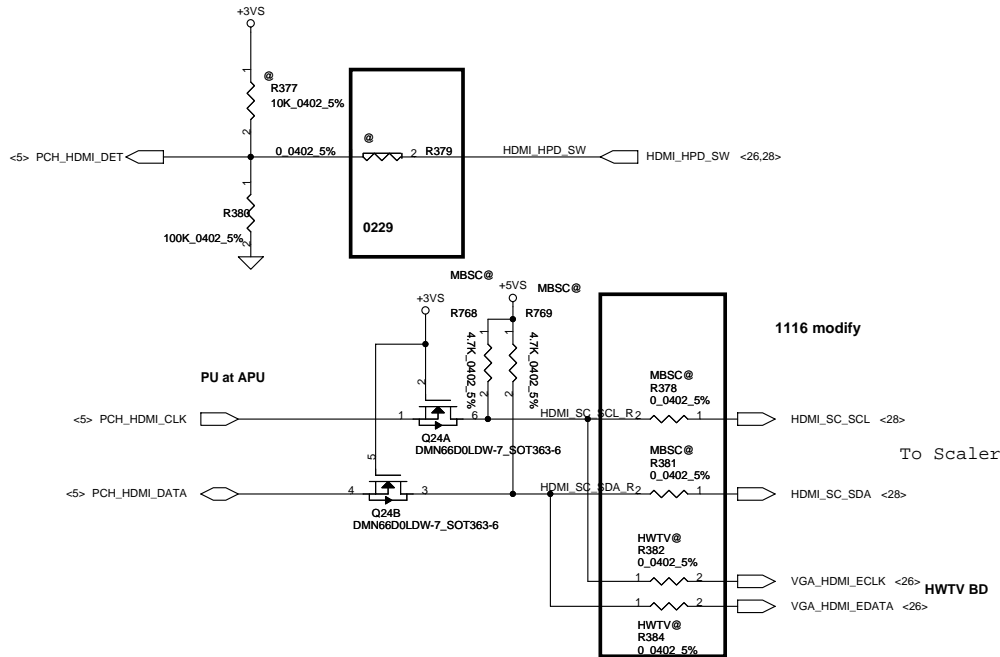


HWTV BD

To Scaler



0912



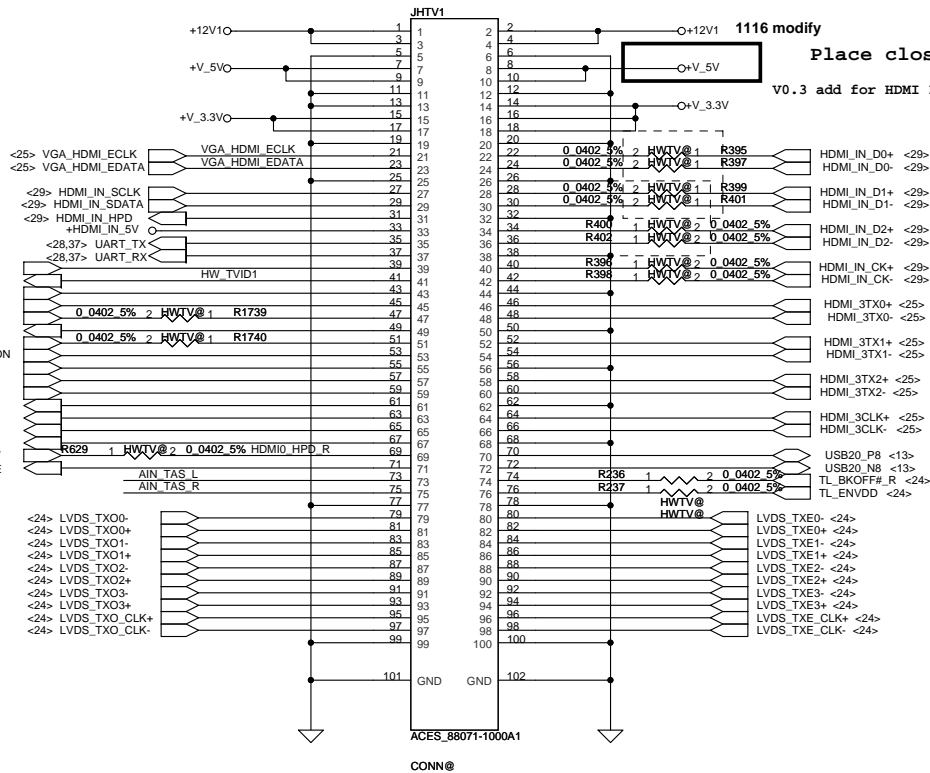
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Source

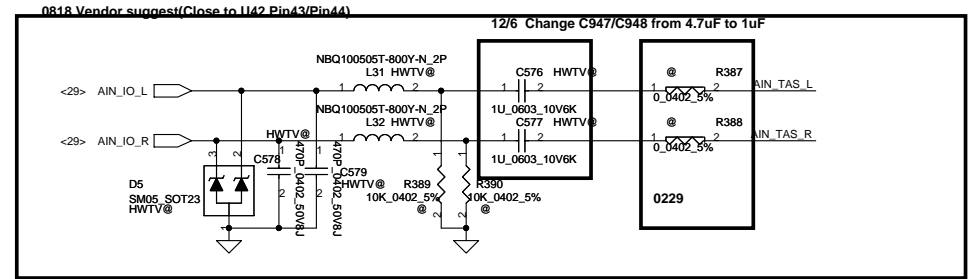
HW_TV_ID1
GPIO_1
GPIO_2
TV_ON#

EC_HWTW_POWER_ON

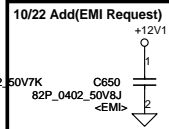
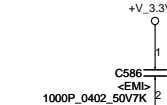
<37> SOURCE#
<37> HW_TV_ID1
<28,37> TV_GPIO1
<28,37> TV_GPIO2
<37,41> CIR_IN
<37> TV_ON OFF
<37> TUNER_PWR_ON
<37> EC_HWTW_PWRON
<28,37> TV_GPIO3
<29> CVBS_L
<29> AGND_CVBS
<36> TV_AMP_OUT_R
<36> TV_AMP_OUT_L
<35> TV_HP_OUT_R
<35> TV_HP_OUT_L
<25,28> HDMI_HP_SW
<36,37> TV_AMP_MUTE



0919 Change symbol of J4 from SP010011B00(88pin to 100pin)ACES_88079-1000A1



10/27 Add C558-C561(EMI request)

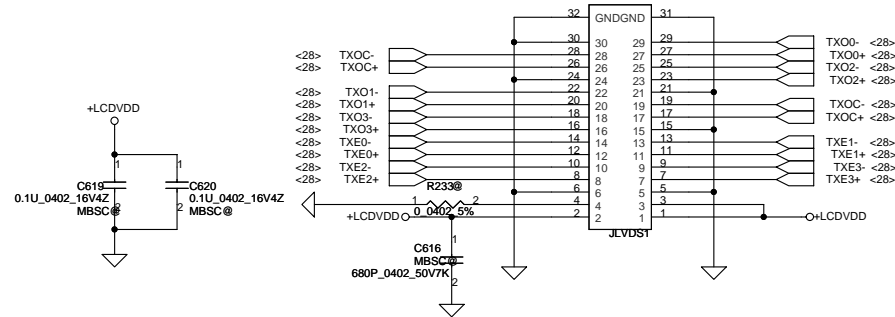


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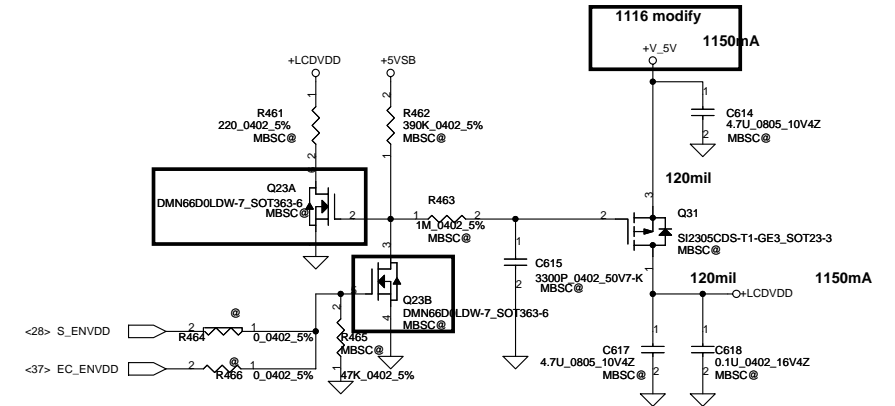
LVDS CONN

CONN@

ACES_88107-30001



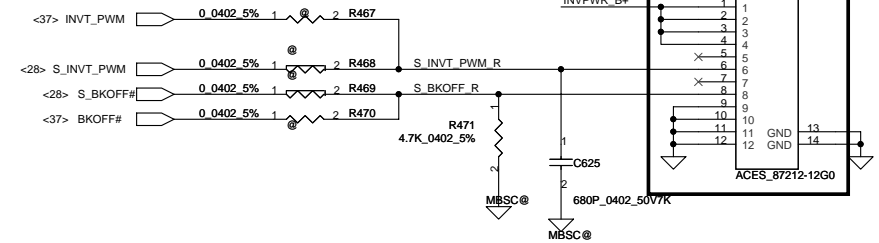
LVDS POWER



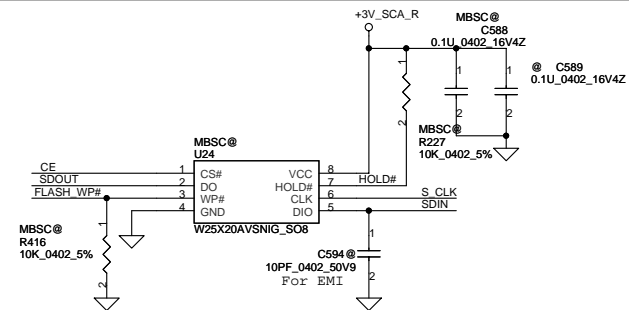
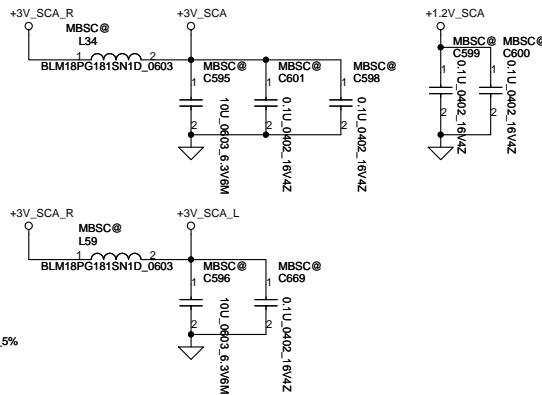
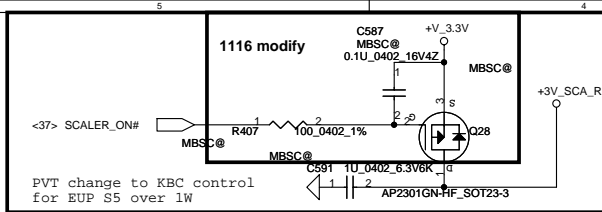
Converter



INVT_PWM: scalar-> converter BKOFF#: scalar-> converter

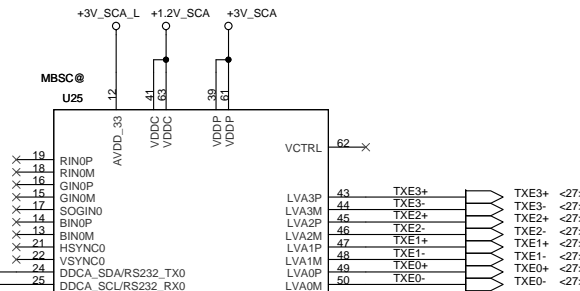
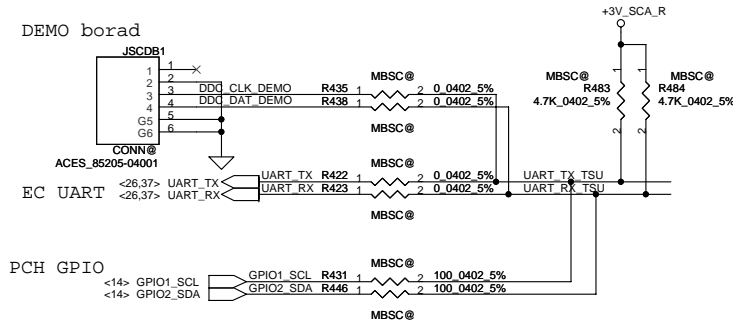


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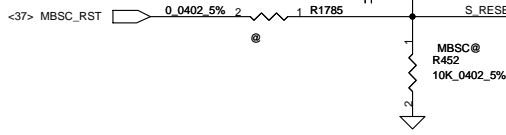
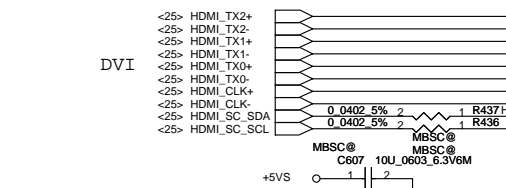
FOR Scalar Firmware Code

DEMO board

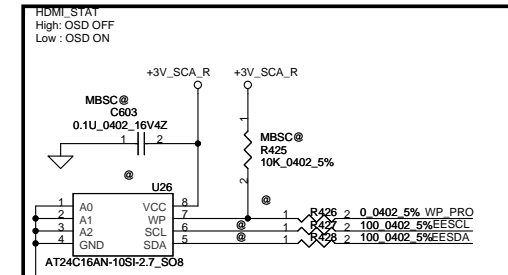
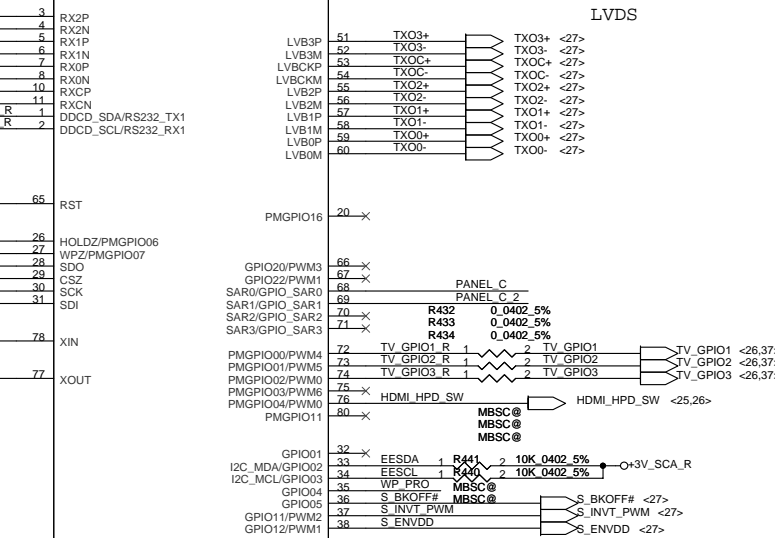
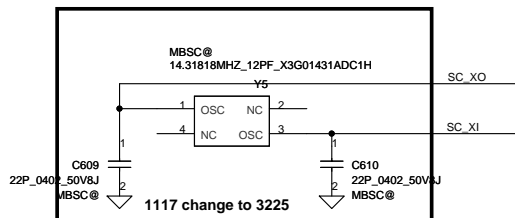


LVDS

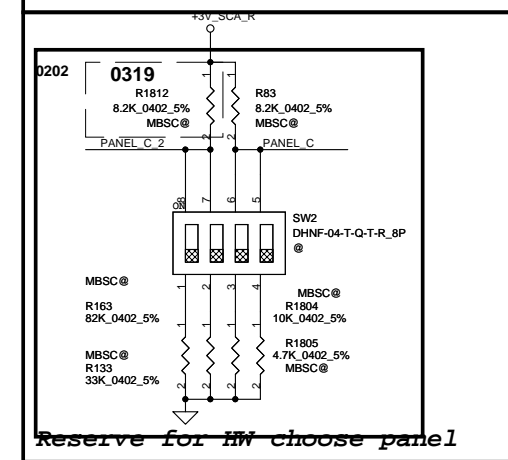
DVI



close to U25 (Scaler)



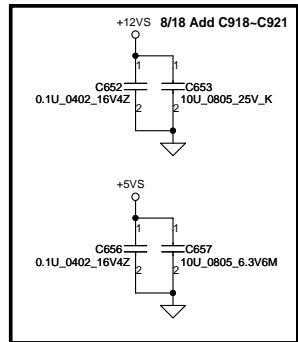
FOR OSD/HDCP Parameter Value



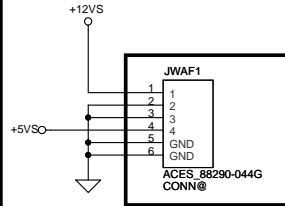
Reserve for HW choose panel

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HDD POWER Conn



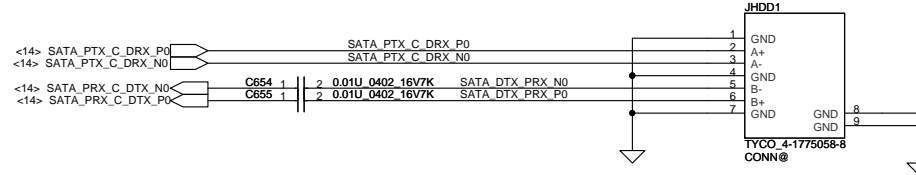
HDD



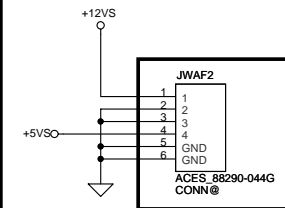
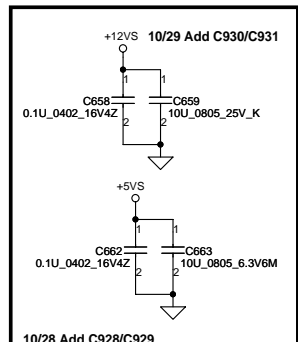
12/6 Change footprint of JWAFF1 from SP02000AO00 to SP02000EB00

Layout Note: Place C918/C919/C920/C921 close to JWAFF1

SATA HDD Conn.



ODD POWER Conn



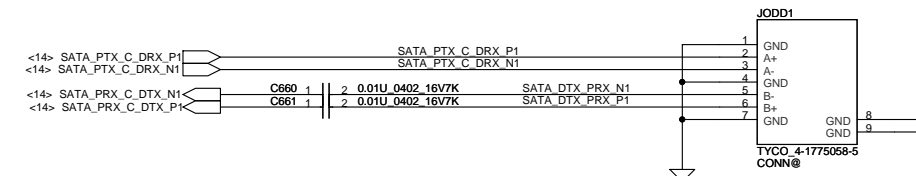
12/6 Change footprint of JWAFF1 from SP02000AO00 to SP02000EB00

10/28 Add C928/C929

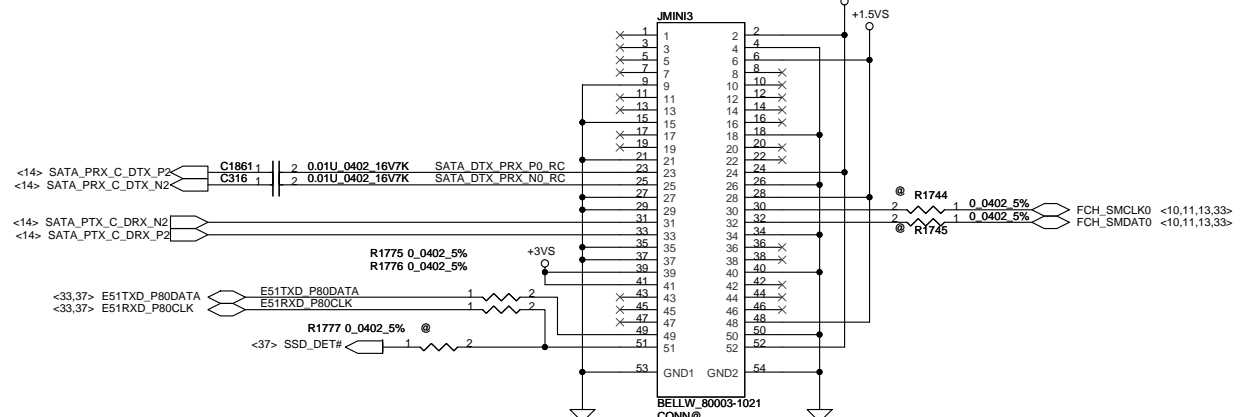
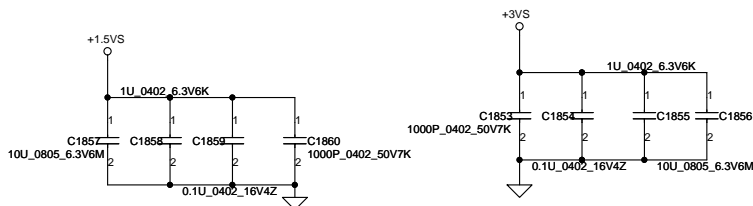
Layout Note: Place C928/C929 close to JWAFF2

ODD

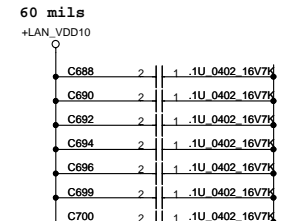
SATA ODD Conn.



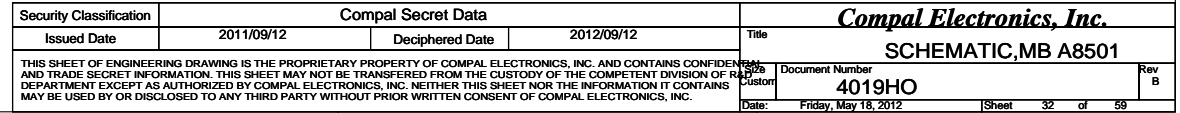
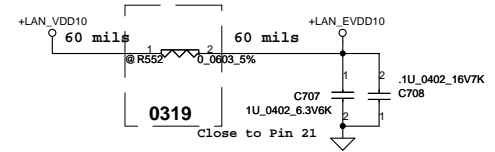
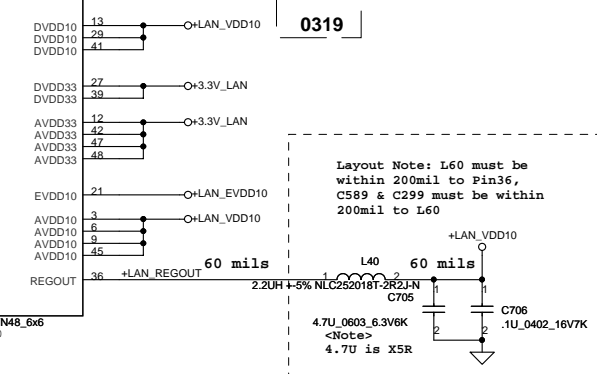
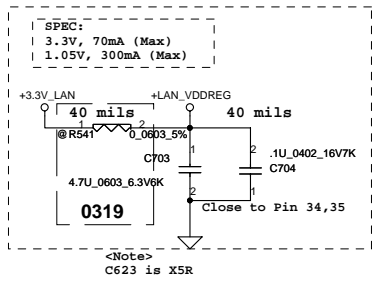
MINI SSD Conn.



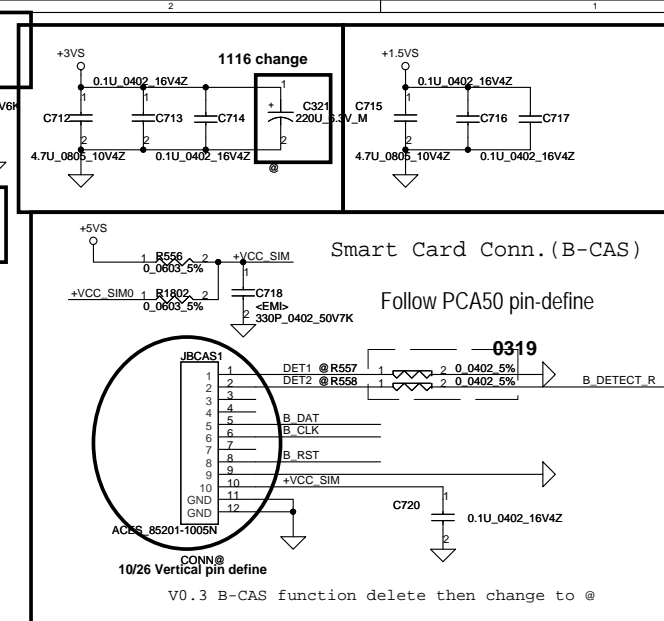
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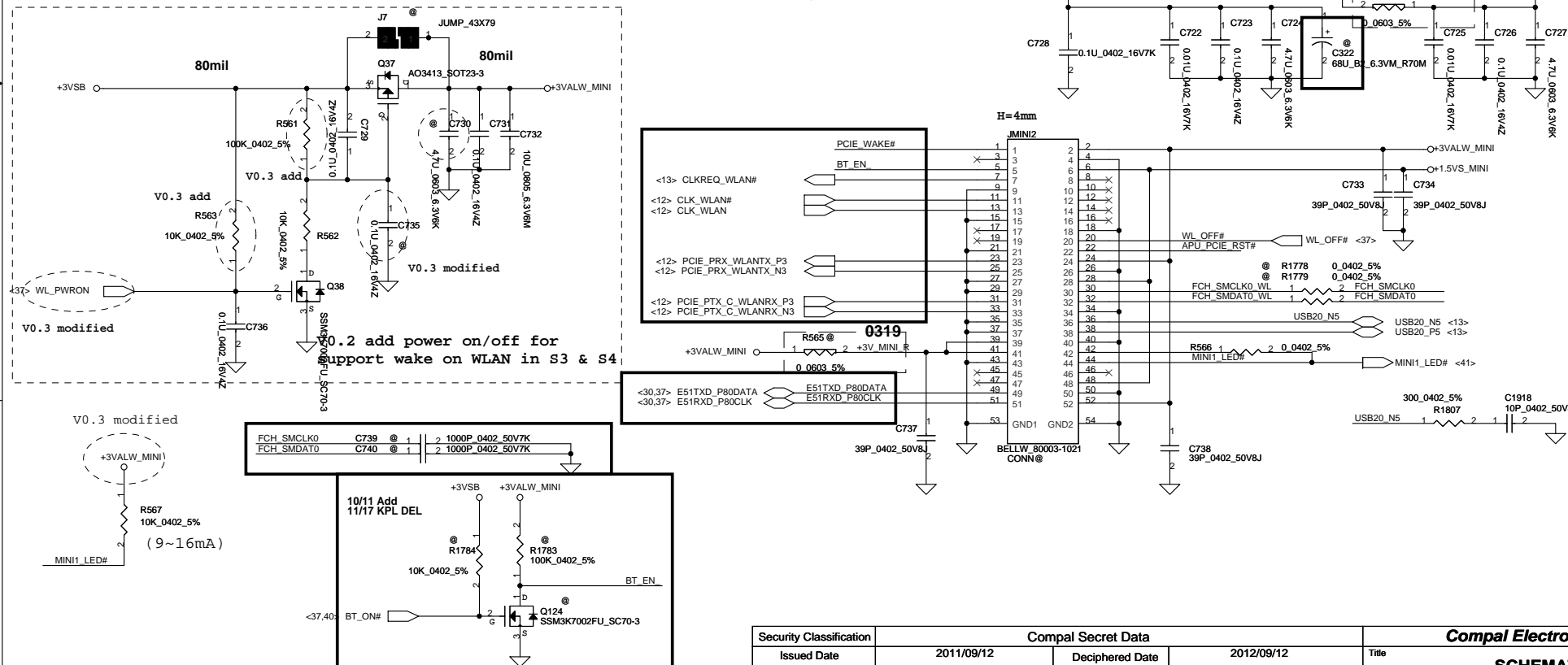
C615, C614, C622, C620, C616, C611, C624 close to pin 3, 6, 9, 13, 29, 41, 45, respectively



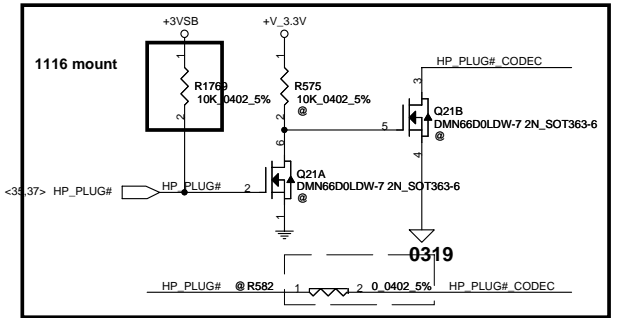
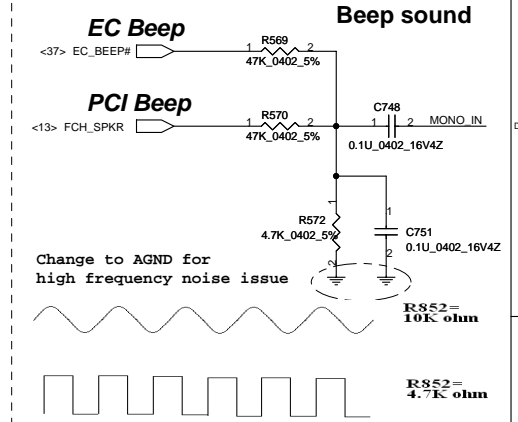
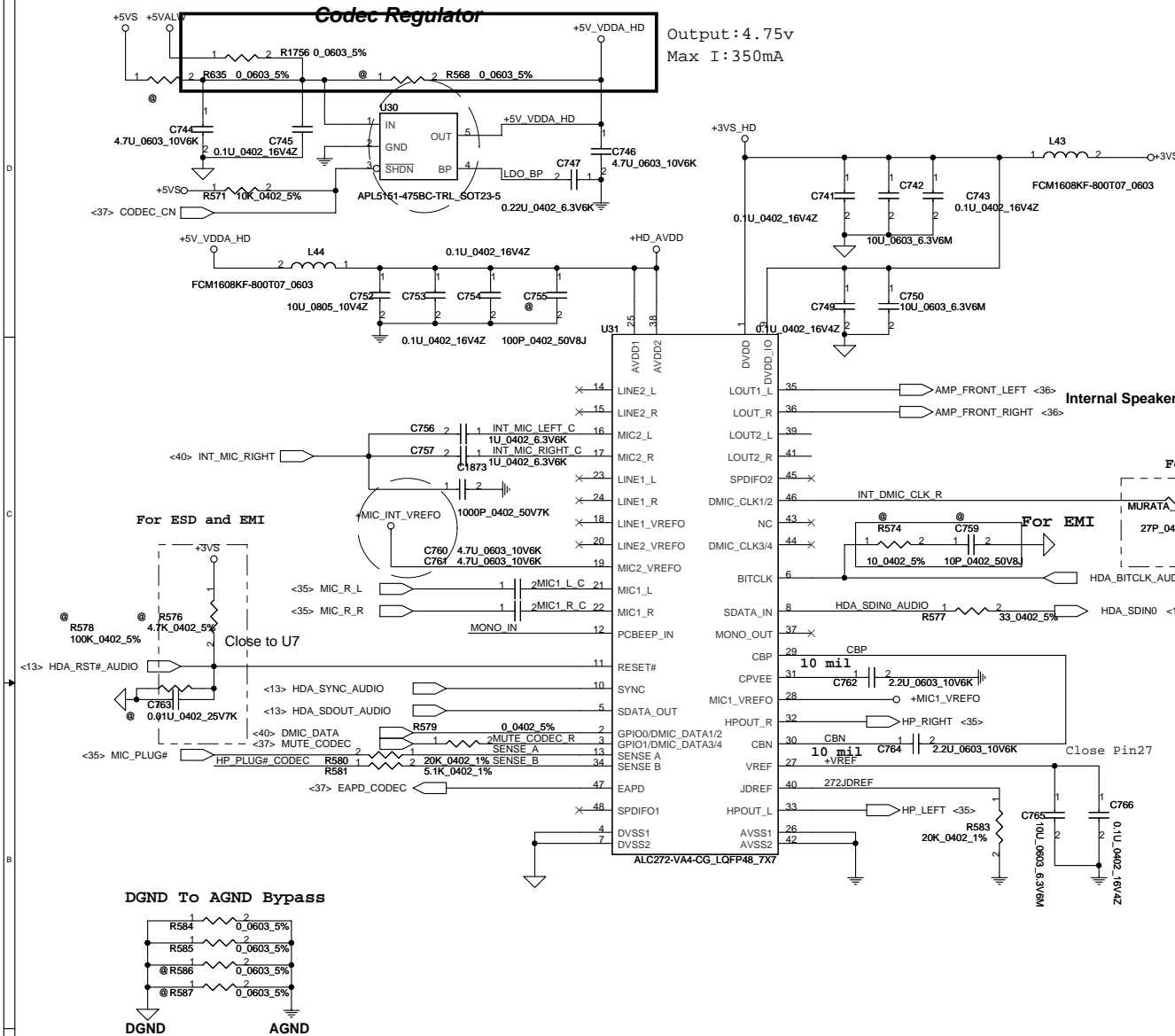
Mini Card Slot 1---TV tuner Current: 3.3 : 2750mA, 1.5: 500mA



Mini Card Slot 1--- WLAN Current: 3.3 : 800mA,



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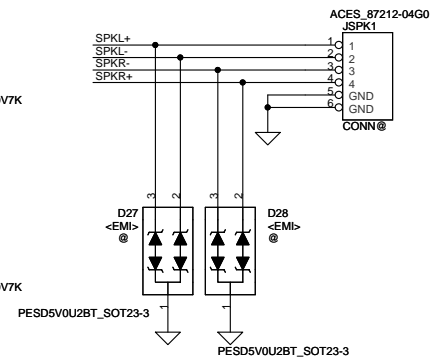
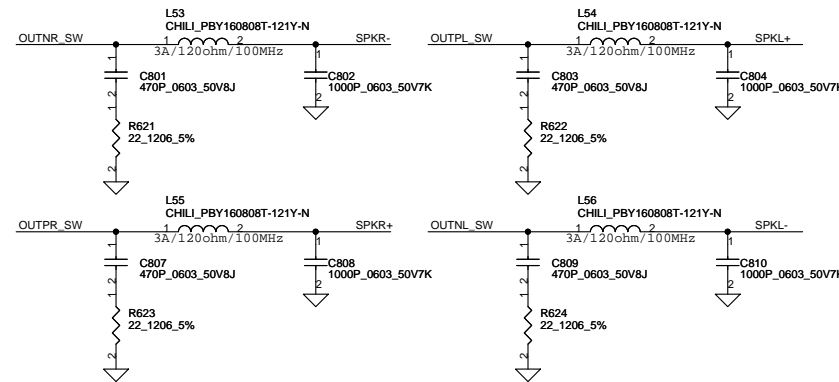
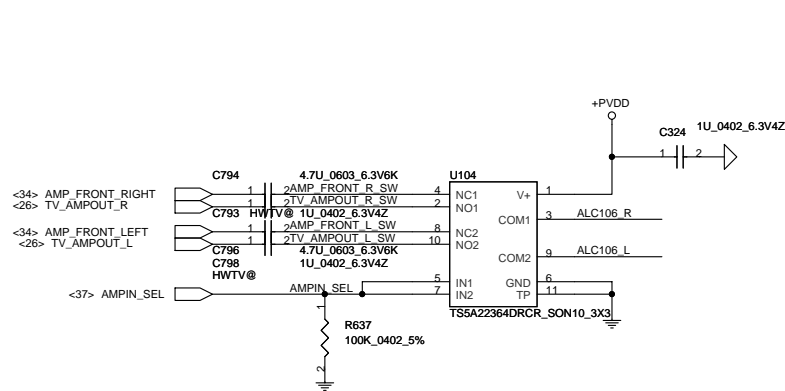
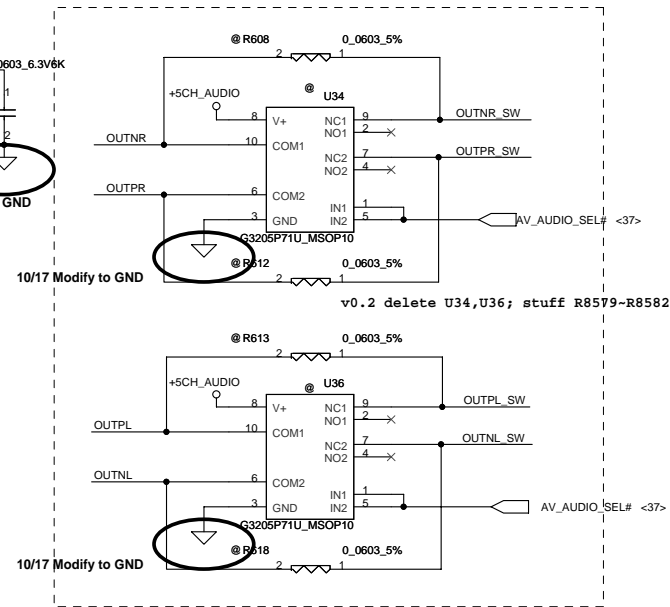
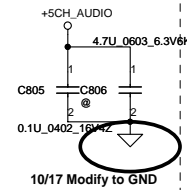
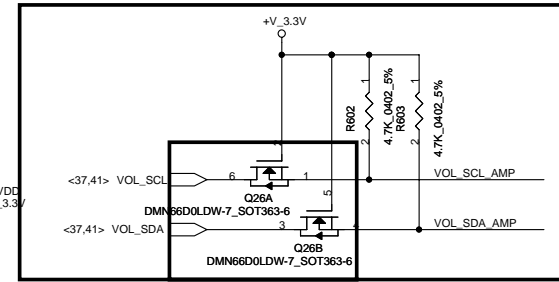
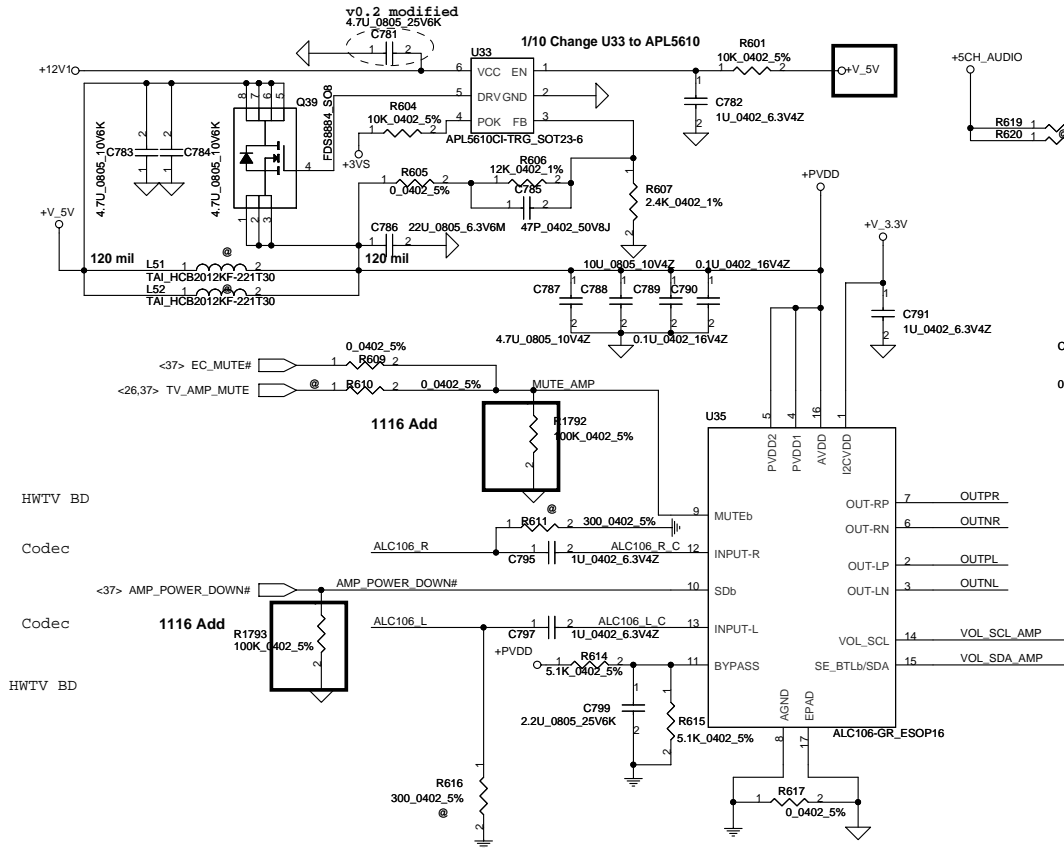


Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	LOUT2 (PIN 39, 41)
	20K	MIC1 (PIN 21, 22)
	10K	LINE1 (PIN 23, 24)
	5.1K	LOUT1 (PIN 35,36)
SENSE B	39.2K	LINE2 (PIN 14, 15)
	20K	MIC2 (PIN 16, 17)
	10K	
5.1K		HP_LUT (PIN 32, 33)

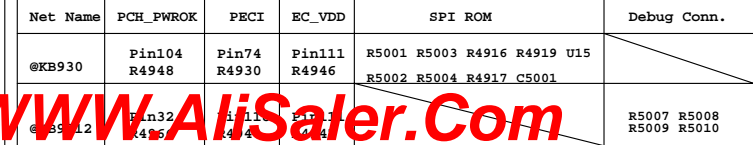


WWW.AliSaler.Com

Vo=0.8(1+R606/R607)
Output:4.8V
Max I:7.5A

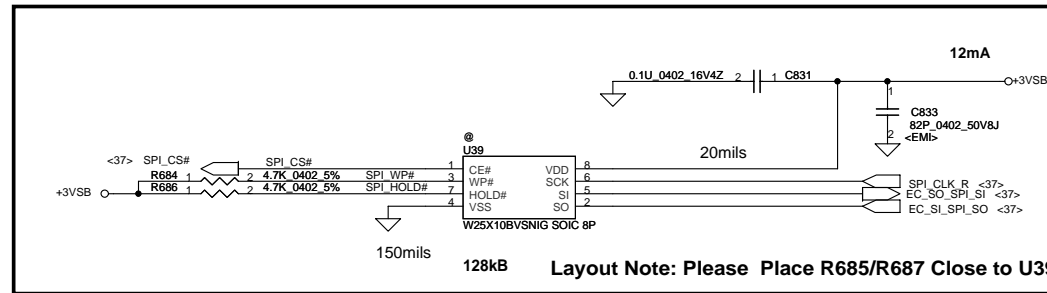
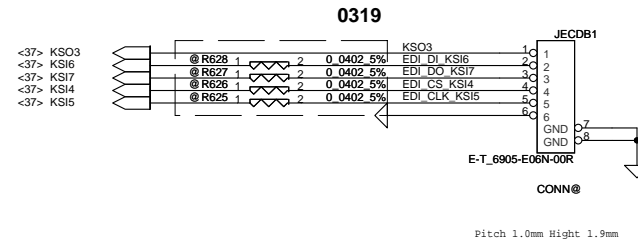


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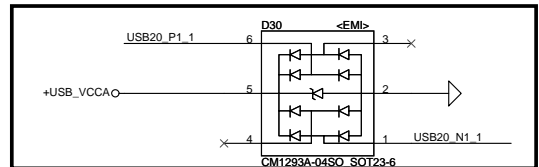
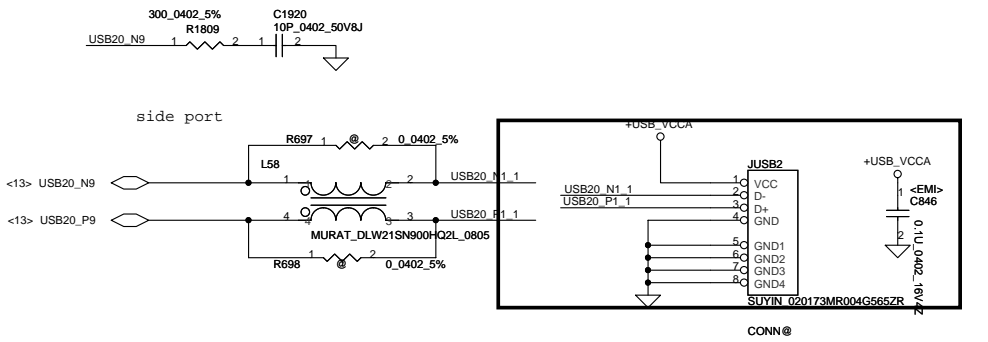
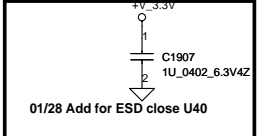
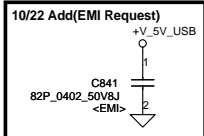
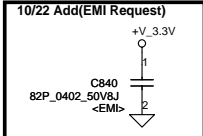
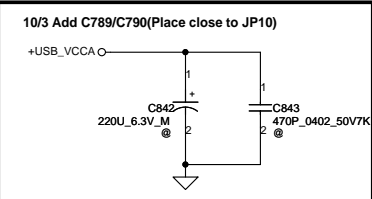
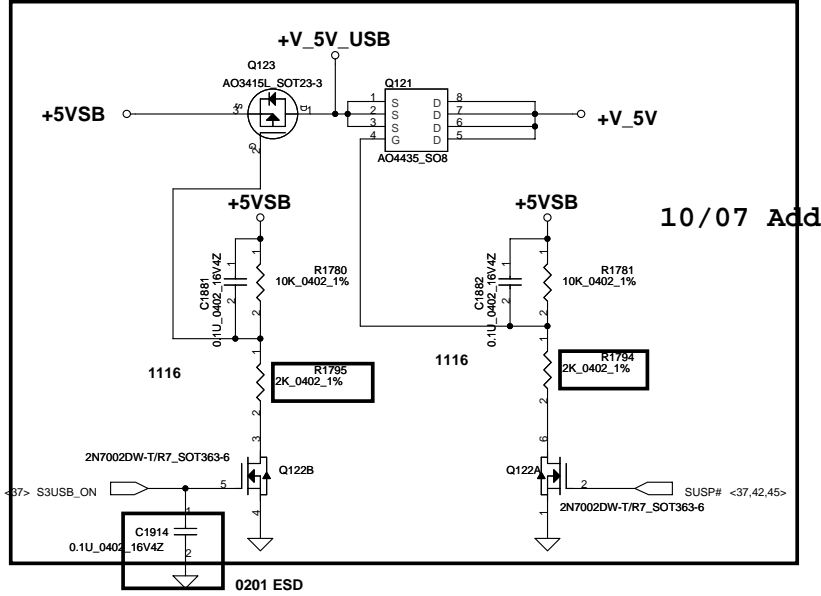
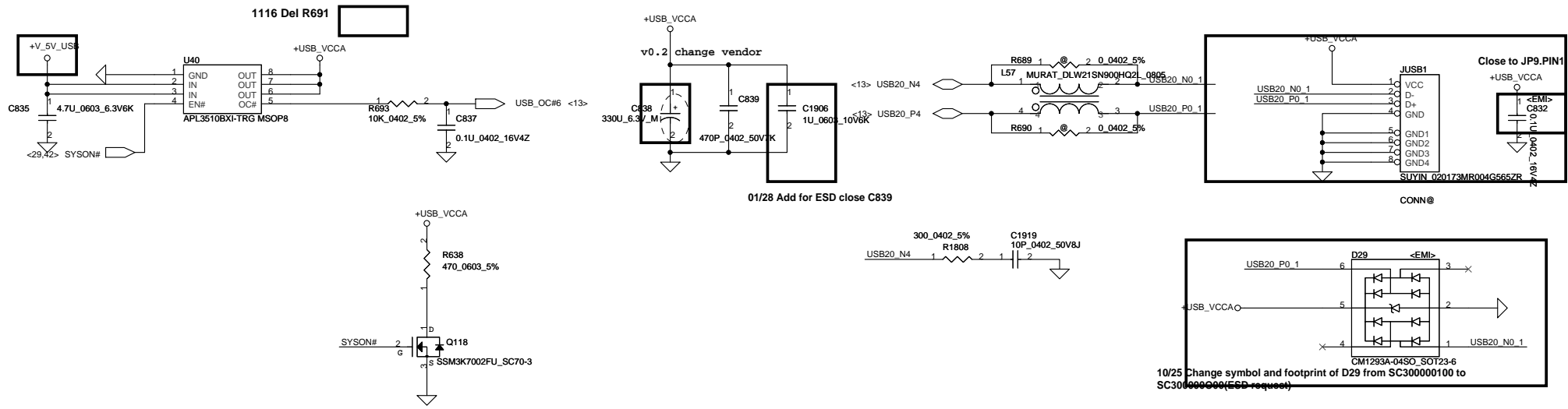


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EC DEBUG CONNECTOR

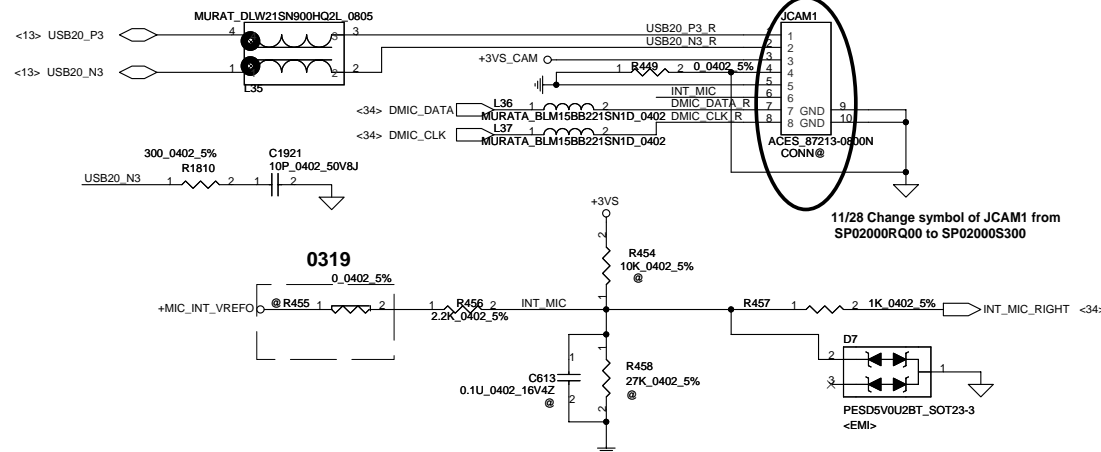
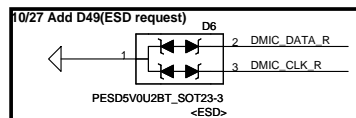
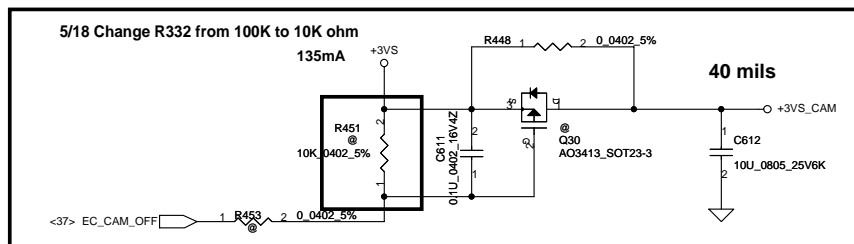


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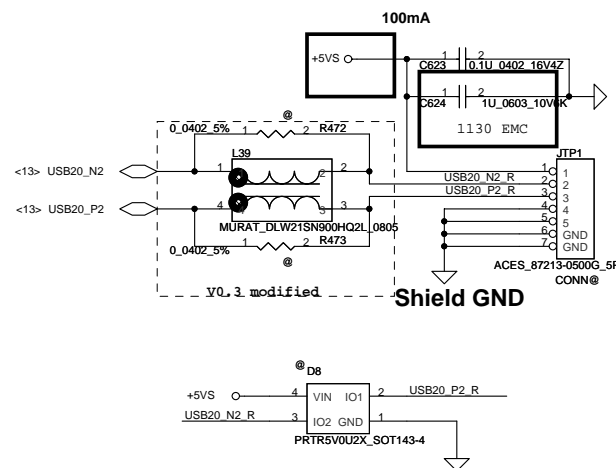
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WebCam+Digital Mic

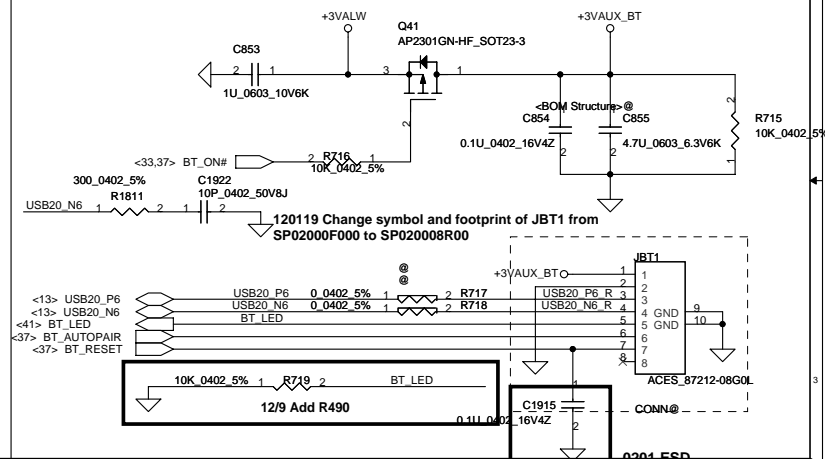


Touch Panel

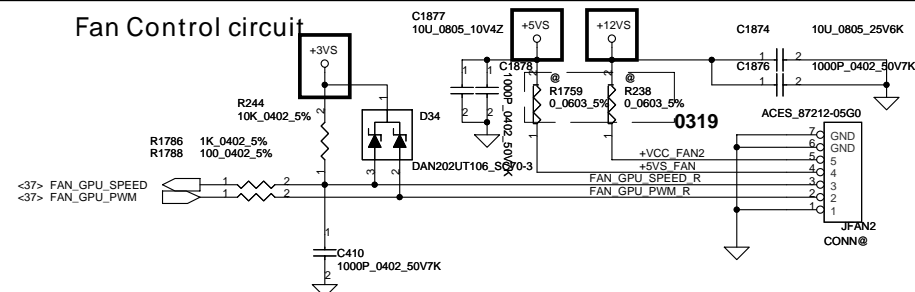
PVT change from alw to vs for EUP.



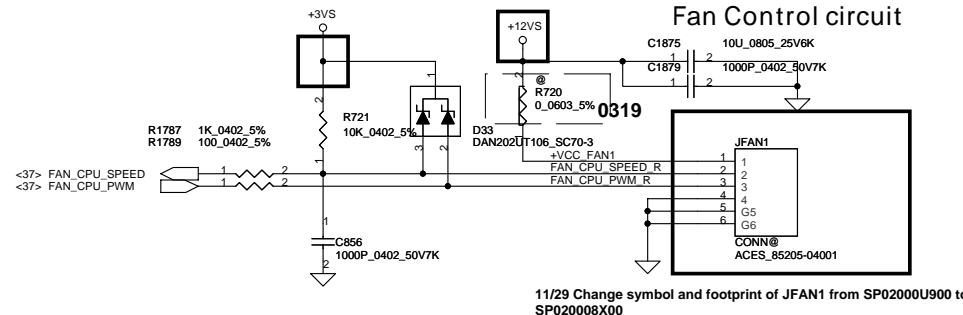
BT Connector



Fan Control circuit

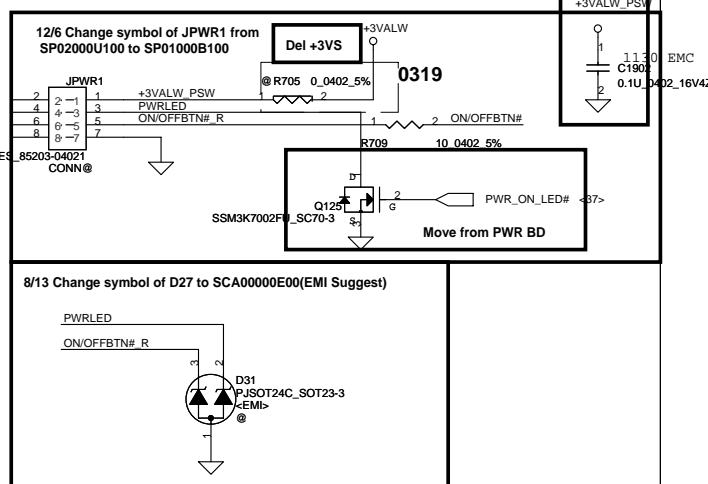


Fan Control circuit

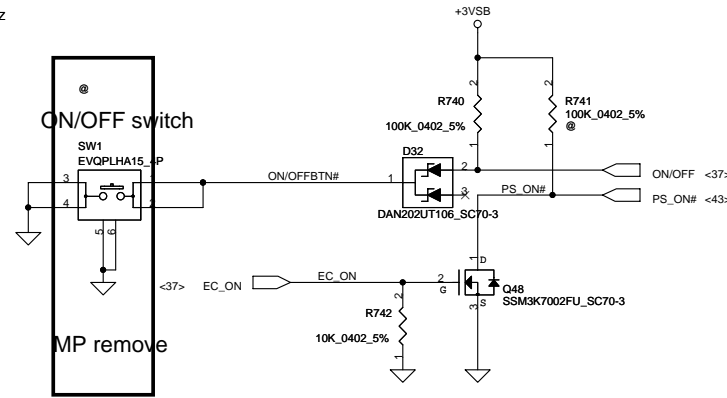


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Date: Friday, May 18, 2012				Rev B

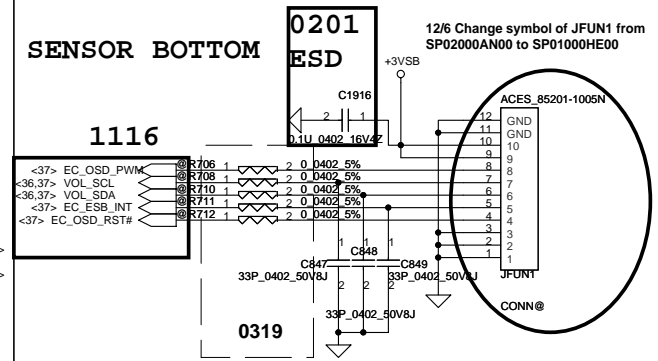
Power switch board



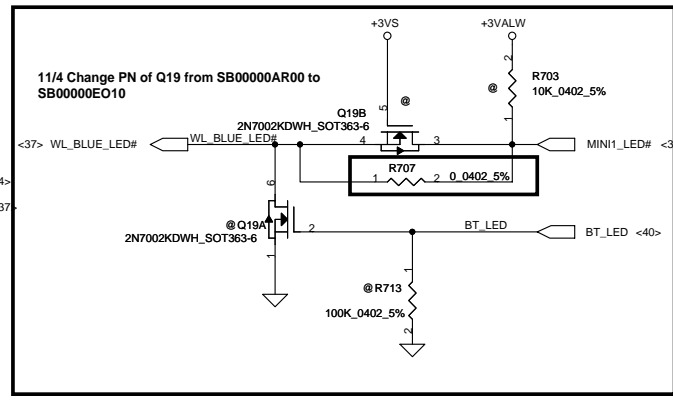
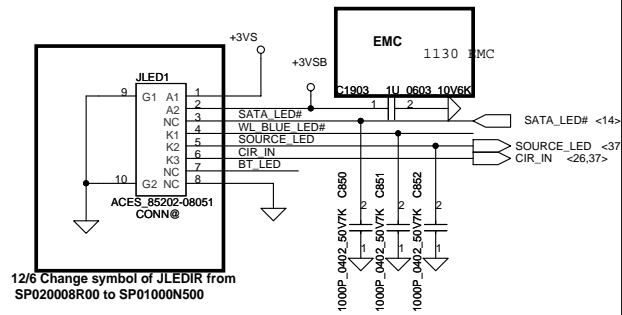
Power Button



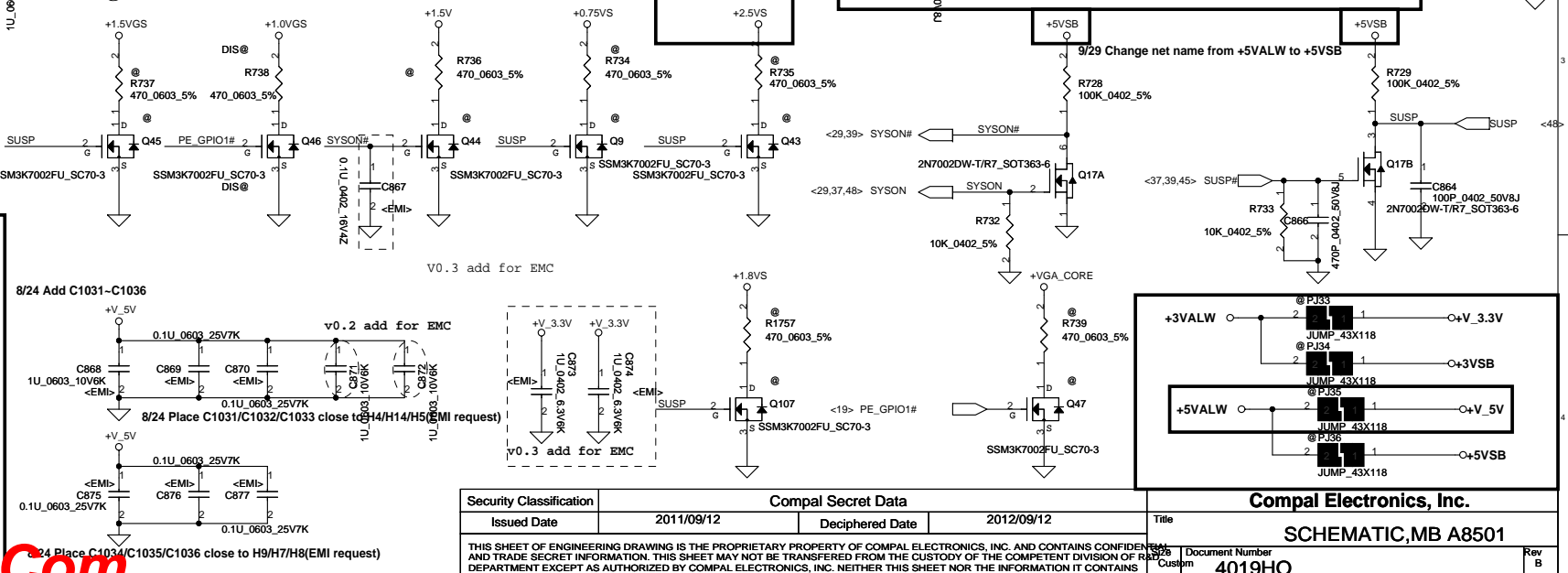
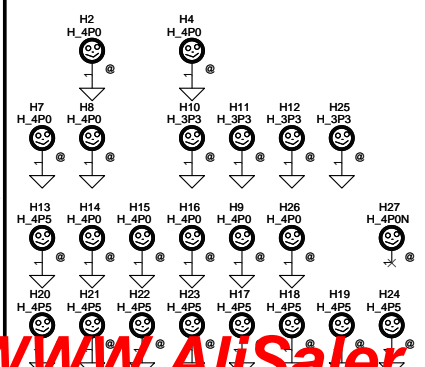
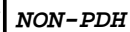
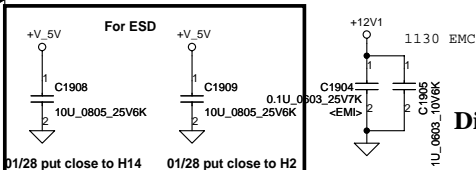
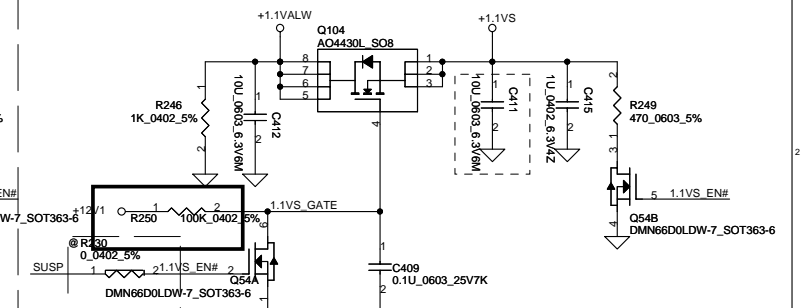
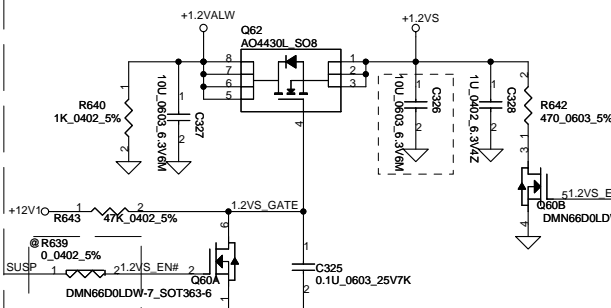
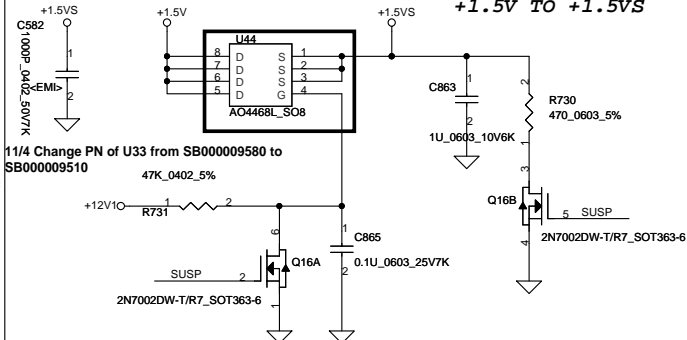
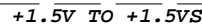
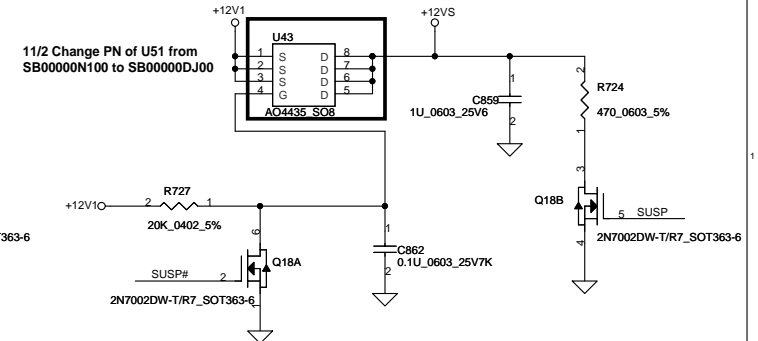
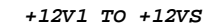
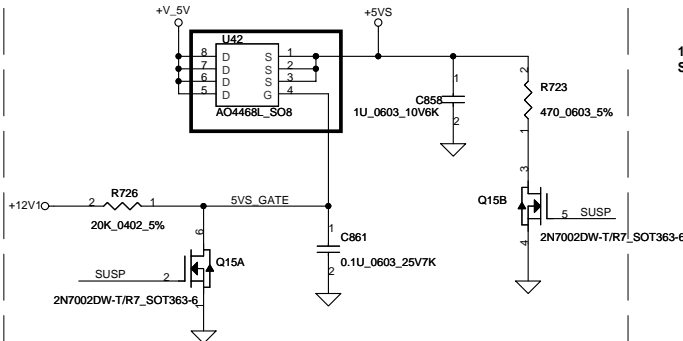
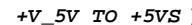
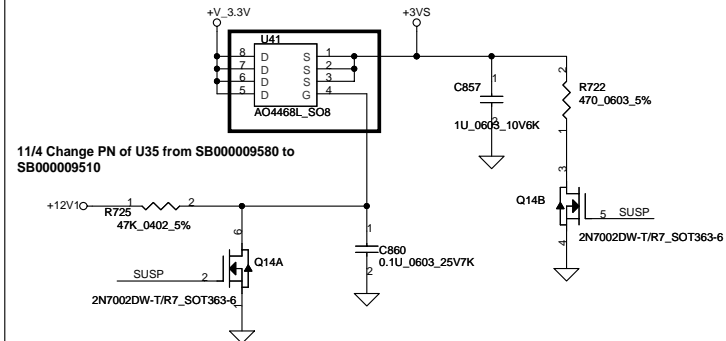
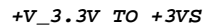
SENSOR BOTTOM



LED board conn.



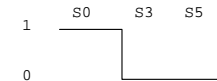
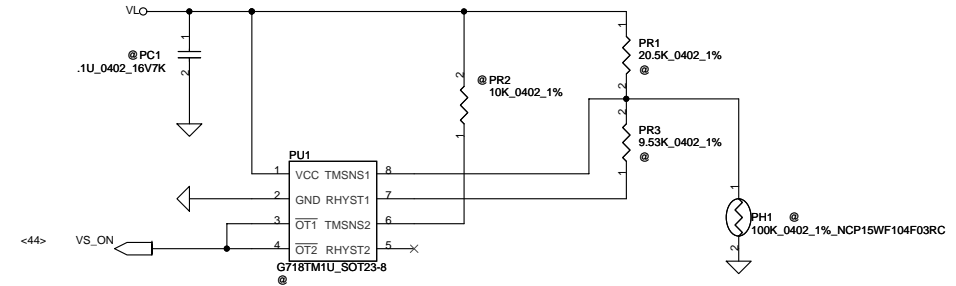
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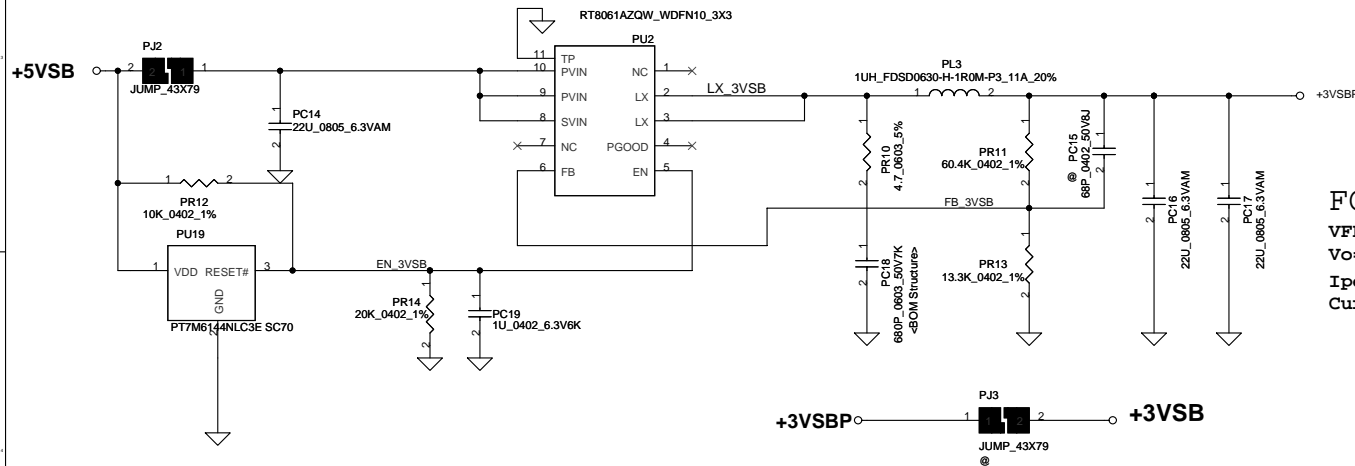
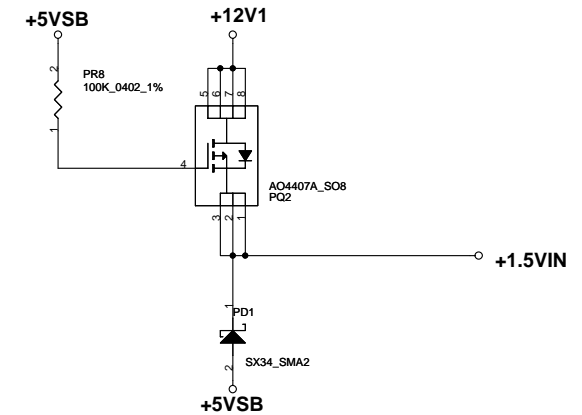
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Title		<div style="text-align: center;"> SCHEMATIC, MB A8501 </div>	
IDENTIFICATION OF RADIO INS	PART 1300 Custom	Document Number <div style="text-align: center;"> 4019HO </div>	Rev <div style="text-align: center;"> B </div>

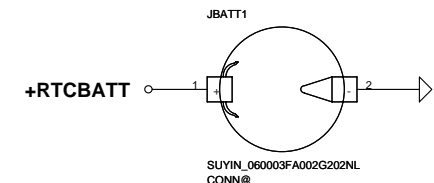

```
CPU thermal protection at 92 degree C
Recovery at 57 degree C
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S3 EN is LOW

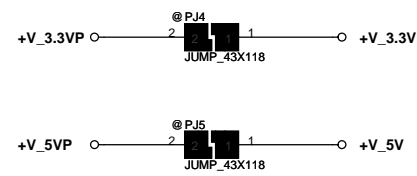
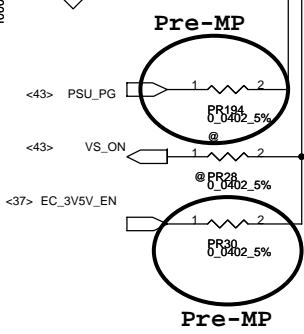


Current limit >4A



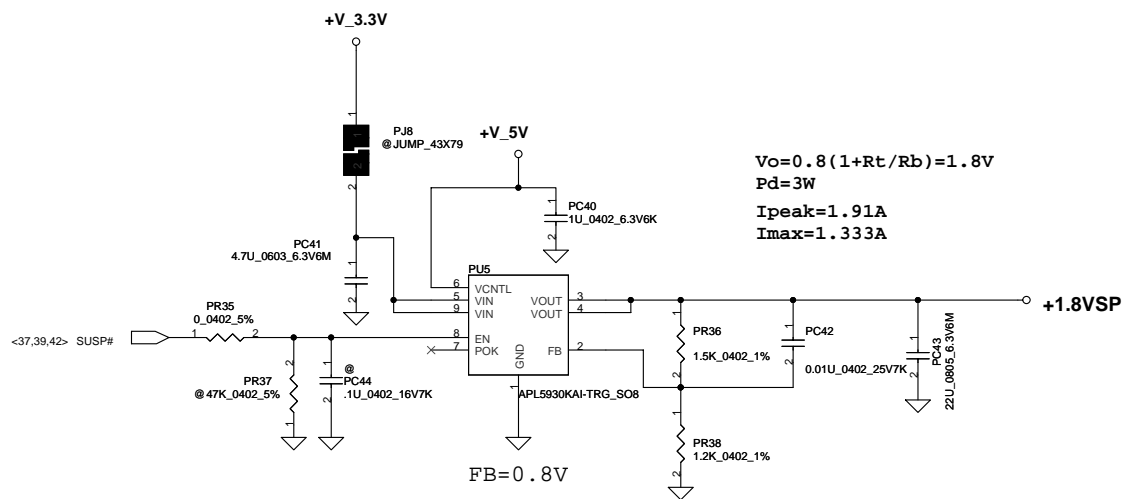
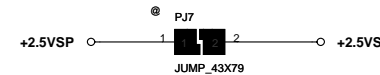
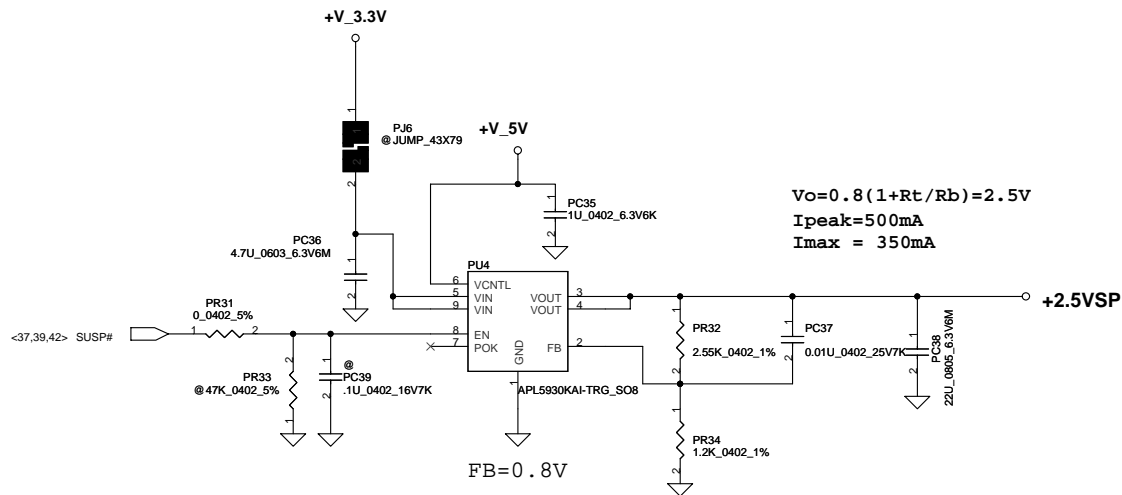
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Cap. ESR=17m
Rds(ON) :Max=15m-ohm
Typ=12m-ohm
Ipeak=3.971A
Imax=2.78A
Iocp=4.765A
fsw=375kHz
Delta I={ (Vin-Vo)/L }*{ (Vo/Vin)*T}=1.357A
Vripple=1.357*17m=23mV
Iocp(set)>4.93A
Vo=2(1+Rt/Rb)=3.337 V
Rt=13.7K, Rb=20.5K
Cap.:LELON
Choke:TOKO 7*7*3
MOS:FAIRCHILD
IC:RICHTEK
Bead:
Diode: PANJIT

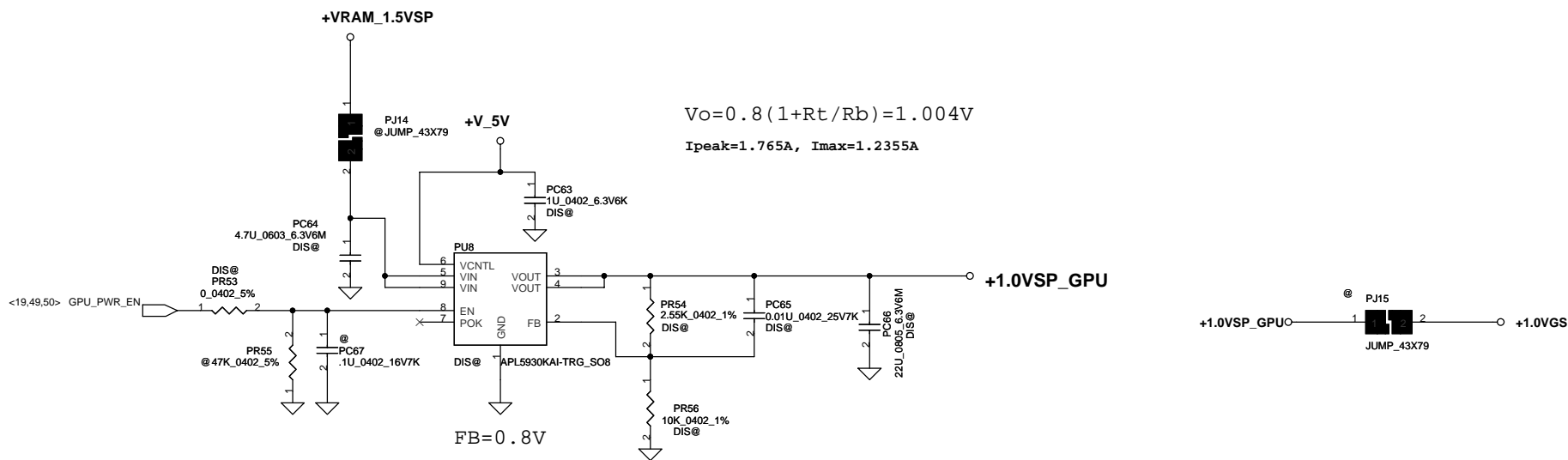
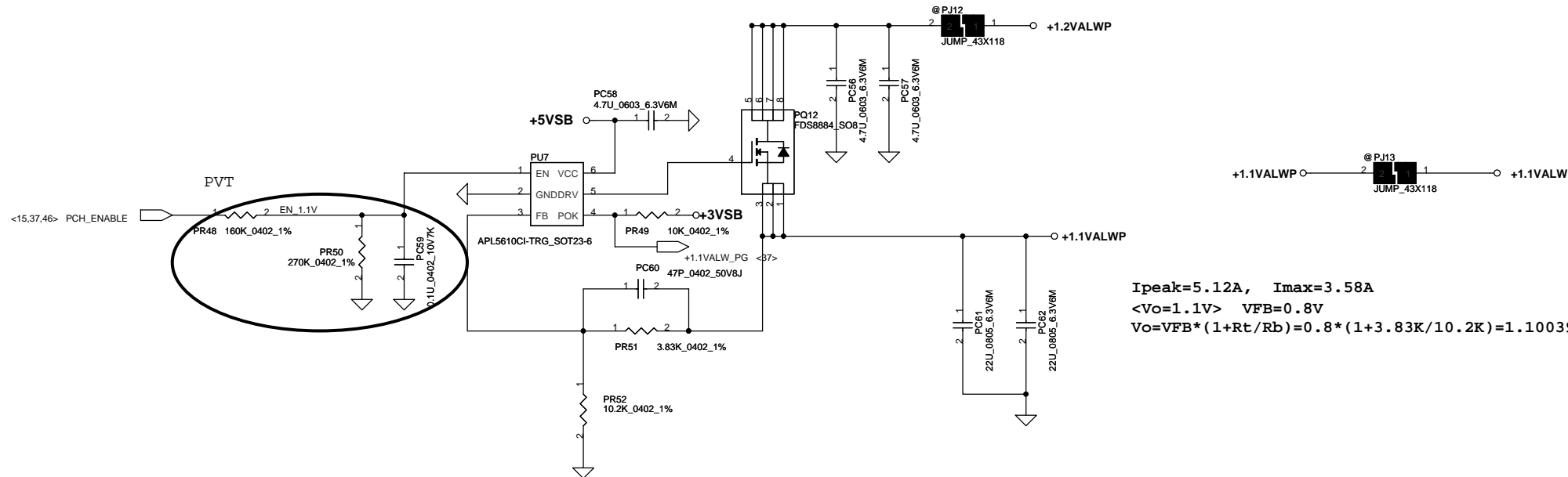


Cap. ESR=17m
Rds(ON) :Max=6.8m-ohm
Min=5.5m-ohm
Ipeak=10.14A
Imax=7.1A
Iocp=12.17A
fsw=300kHz
Delta I={ (Vin-Vo)/L }*{ (Vo/Vin)*T}=4.419A
Vripple=2.068*17m=75.126mV
Iocp(set)>12.2A
Vo=2(1+Rt/Rb)=5V
Cap.:LELON
Choke:Maglayers 7*7*3
MOS:FAIRCHILD

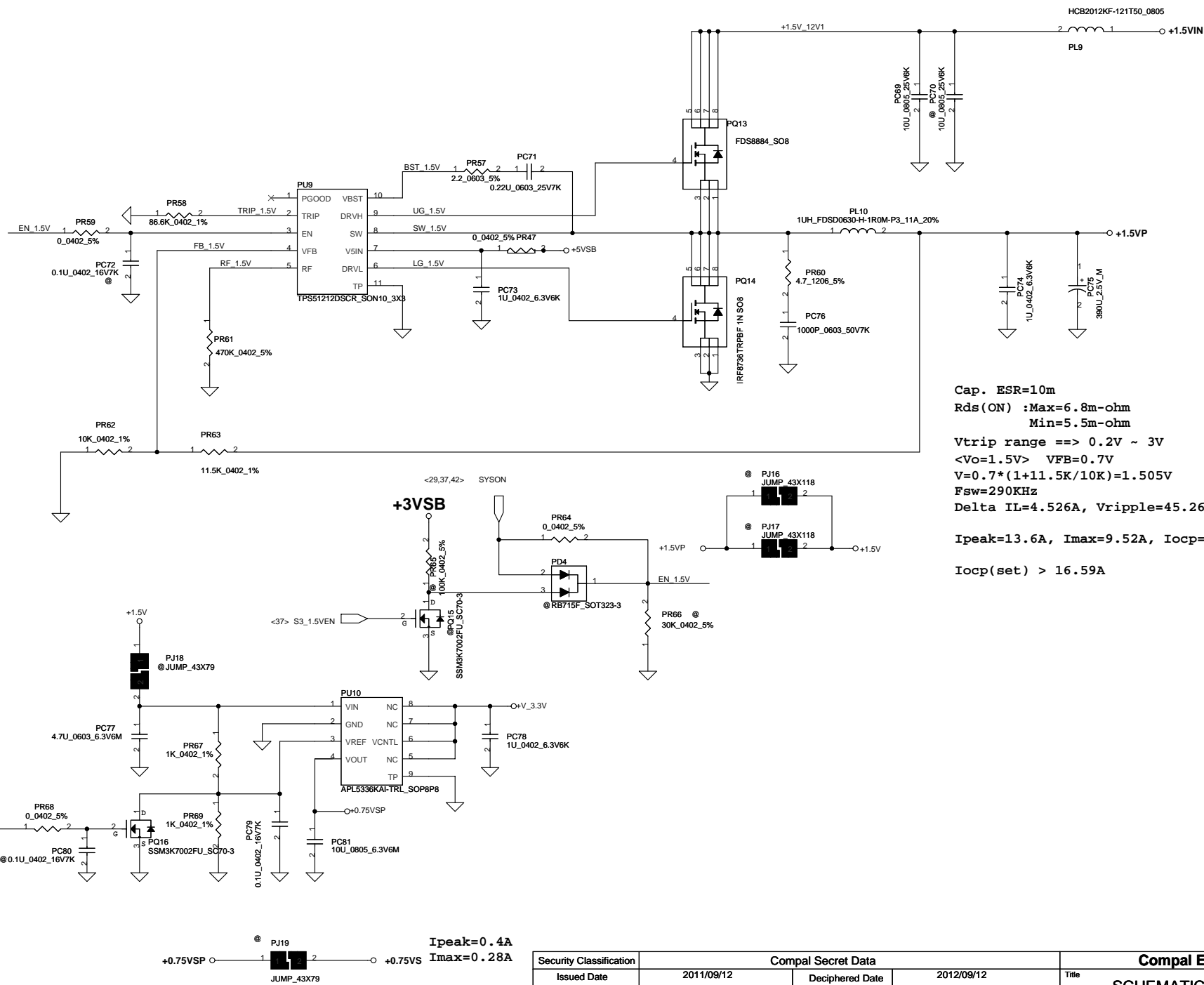
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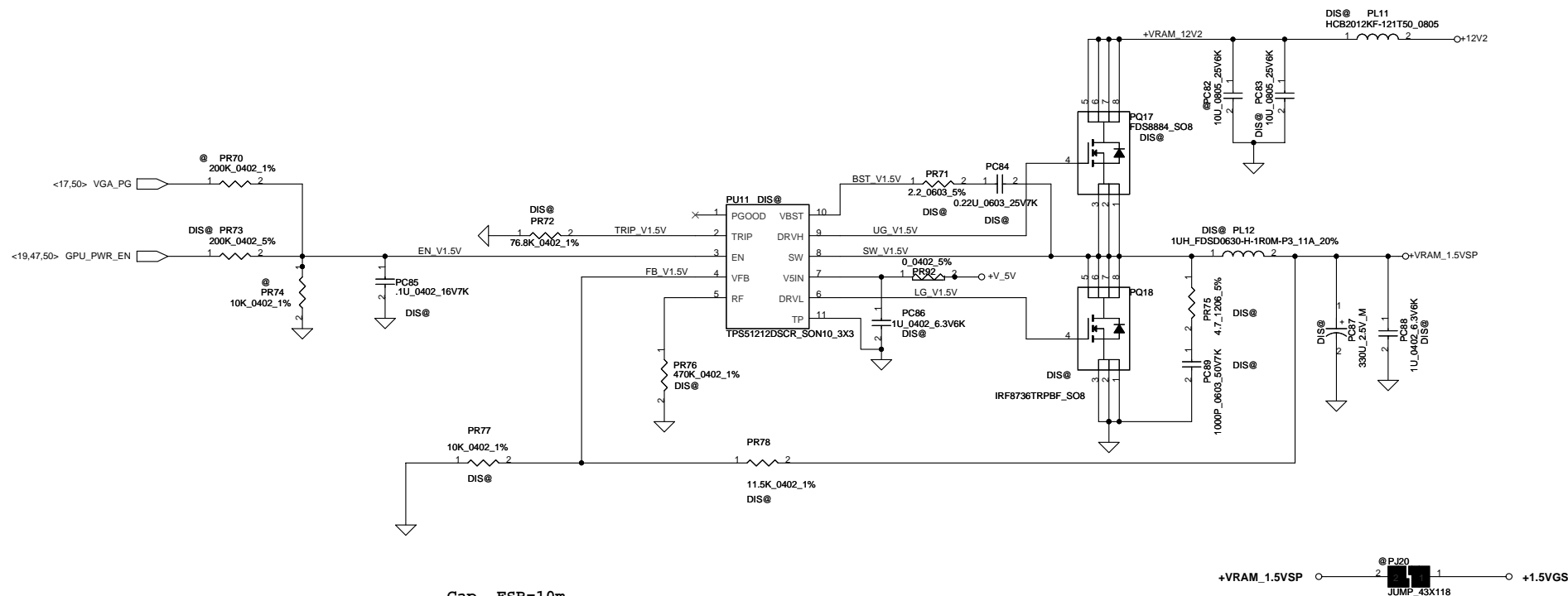
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GPU_VID1	GPU_VID0	VGA_CORE
0	0	0.90V
0	1	0.95V
1	0	1.10V
1	1	1.15V

(Default)

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Cap. ESR=5m

Rds(ON) :Max=3.6m-ohm
Min=3m-ohm

Ipeak=22A, Imax=15.4A, Iocp=1.2*Ipeak=26.4A

Vtrip range ==> 0.2V ~ 3V

<Vo=1.15V> VFB=0.7V

Fsw=290KHz

Delta IL= 9.96A, Vripple=49.798V

Iocp(set) >27.85A

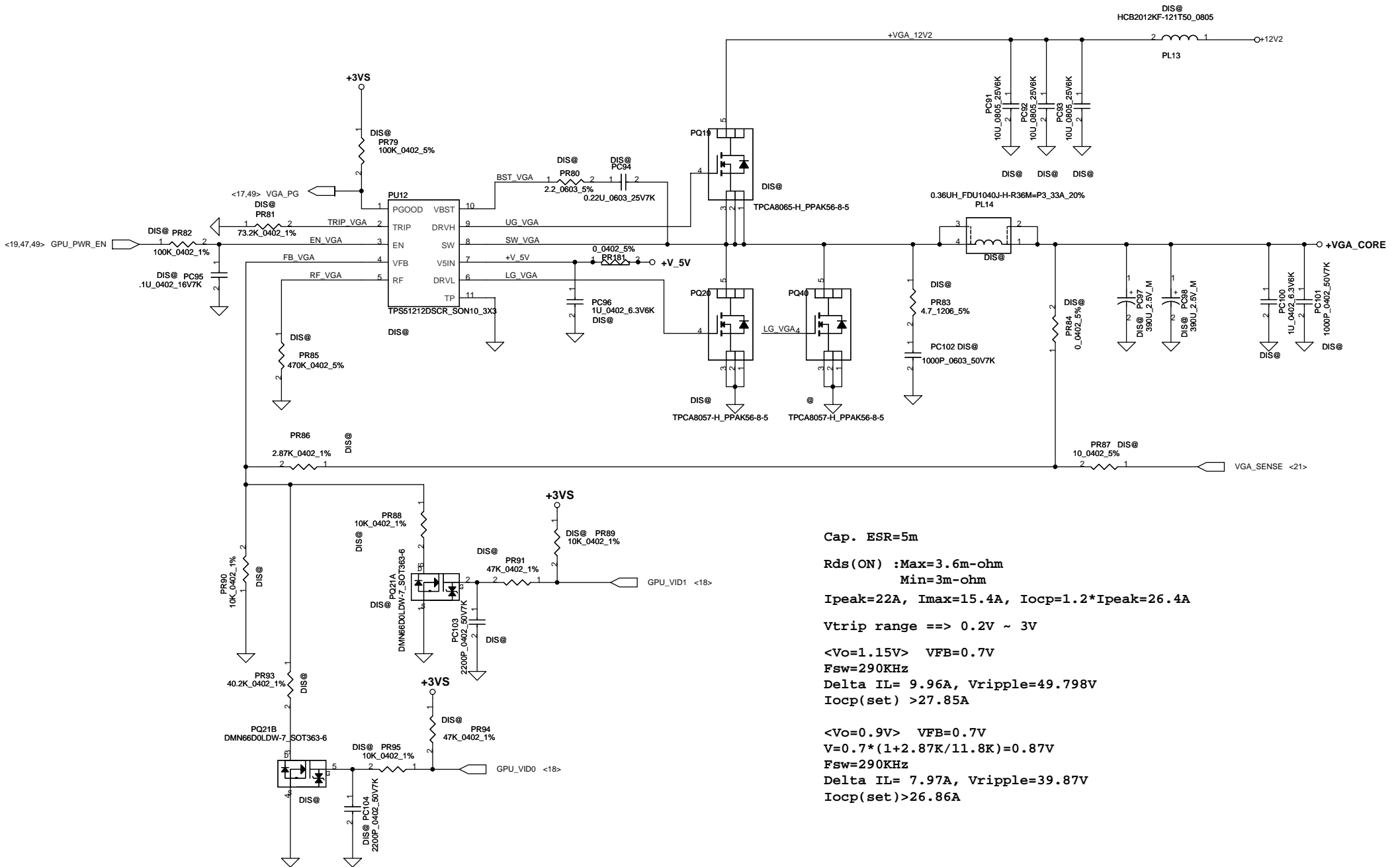
<Vo=0.9V> VFB=0.7V

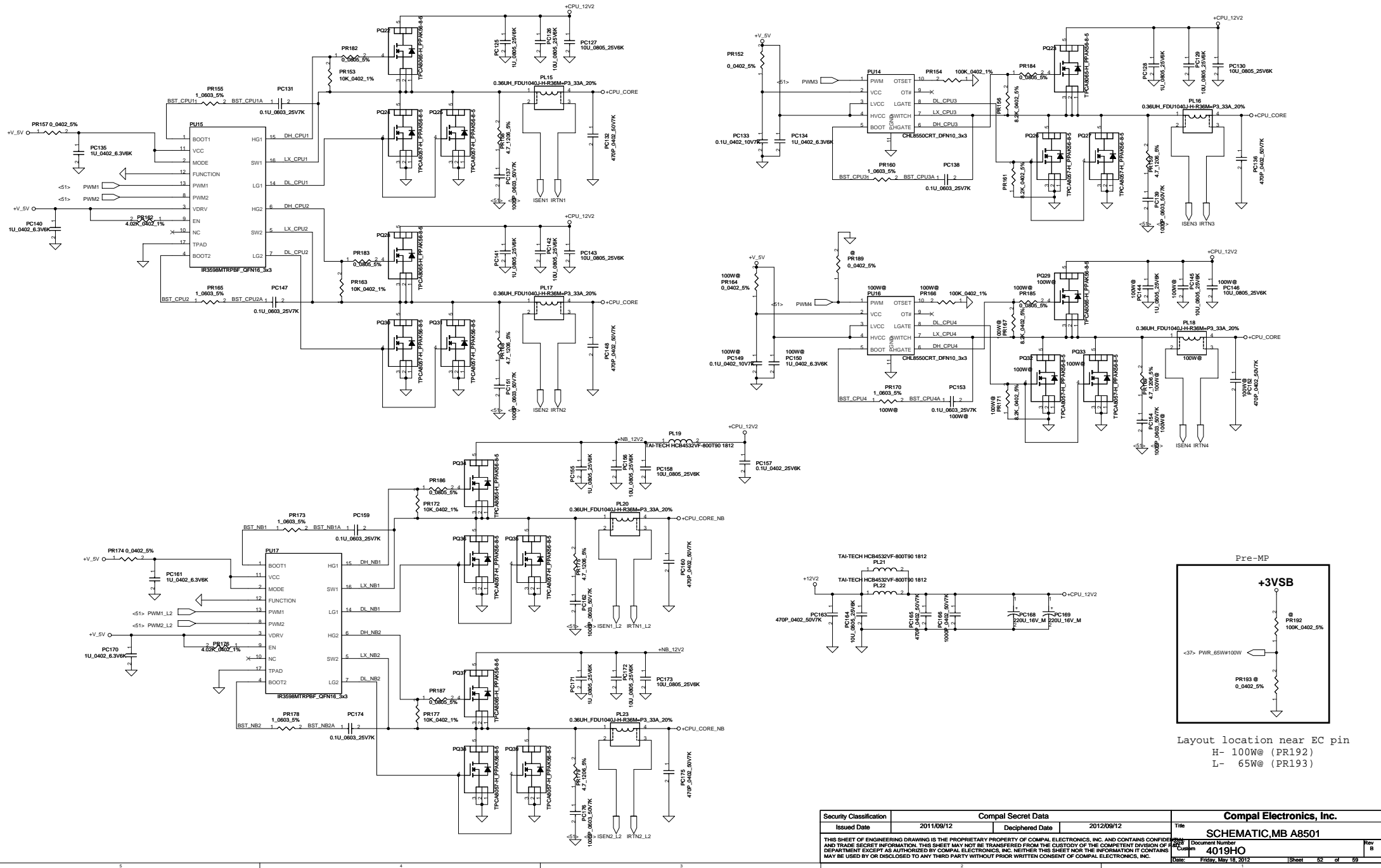
V=0.7*(1+2.87K/11.8K)=0.87V

Fsw=290KHz

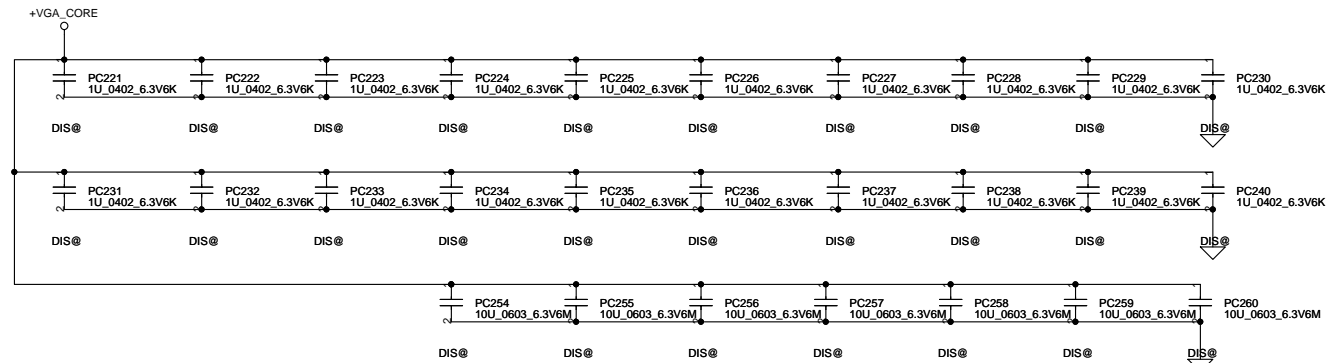
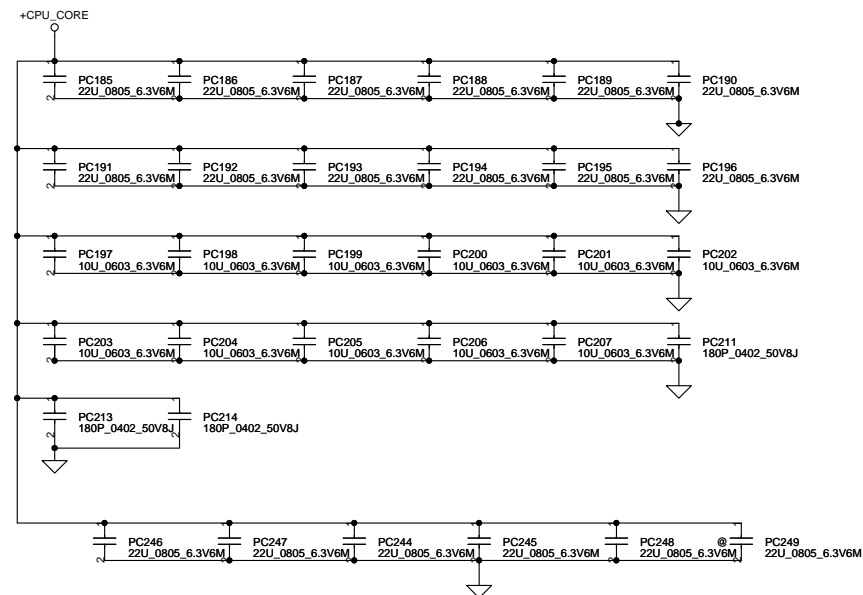
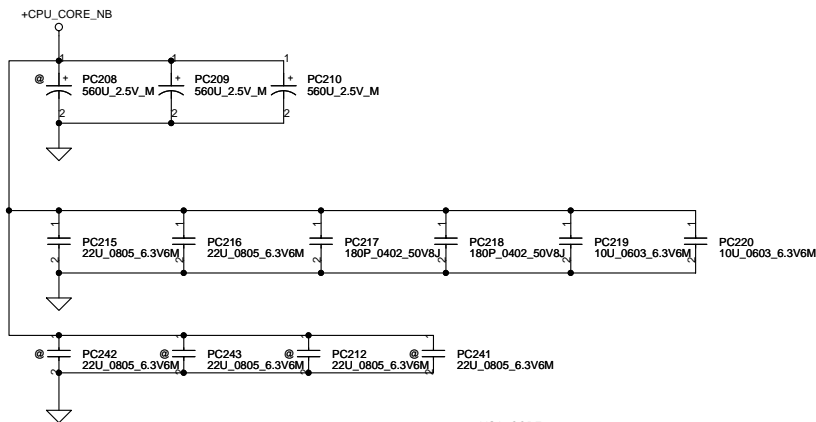
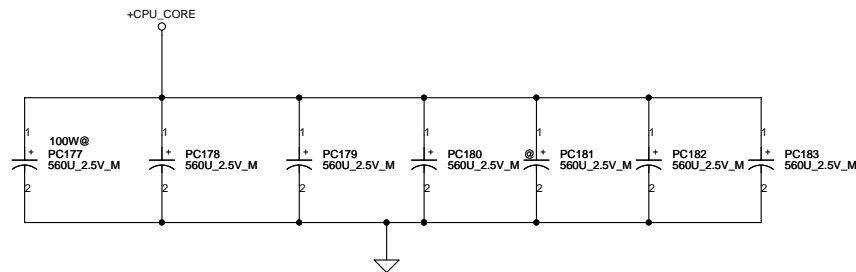
Delta IL= 7.97A, Vripple=39.87V

Iocp(set)>26.86A





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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	2011/9/21	P50	Change PR88 to 10k ohm	Modify VGA_CORE VID setting value
2	2011/9/22	P47/P50	Change RN pin netname to GPU_PWR_RN	For HW request
3	2011/9/27	P50	Change PL14 connection to pin 1 and pin 4	For Layout
4	2011/9/28	P52	Change PC153 PIN2 to LK_CP04	Modify PU16 bootstrap circuit
	2011/9/28	P49/P49/P50	Change +1.2ALMP/+VRAM_1.SVSP/+VGA_CORE input to +CPU_12V2	For layout easily
5	2011/9/28	P50/P52	Change PC90/91/92/93/126/127/129/130/142/143/145/146/156/158/164/172/173 PW from SE14210DMLO to SE00000QK00	For Cost saving
6	2011/9/28	P50/P46	Change PL13/PL7 PW to SM01000C000	For Cost saving
		P51	Net name:+CPU_12V2	
		P50	Remove PC90	For Layout
7	2011/9/28	P43/P46	remove PR9/PQ3/PC9/D31/PR47/PQ11/PC35/D311	For Layout space
8	2011/9/29	P49	change PC87 from 390u/6h to 330u/4.2h	For Layout space
9	2011/10/03	P52	change PR146 PIN1 connect to PR148	IR FAE suggest
10	2011/10/03		change PC20, PC50, PC52, PC73, PC74, PC78, PC86, PC89, PC96, PC150, PC168, PC134, PC135, PC140, PC150, PC168, PC170 to SE000000000	For Cost saving
			change PC25, PC13, PC36, PC41, PC56, PC58, PC64, PC77 to SE10747M80	
11	2011/10/04	P50	add PQ40	co-lay VGA
12	2011/10/04	P52	Modify PU14 and PU16 footprint form QFN10_3*3 to QFN10_3*3	Modify to correct footprint
13	2011/10/05	P50	Connect PL14 PIN2 to PIN1 and PIN3 to PIN4	For Layout shape
14	2011/10/11	P51	Modify PR97, 98, 149, 150 connection	
			Add short pad PR180	IR FAE suggest
15	2011/10/11	P51	Change PR1, PR3, PR4 to SL200001000	For Cost saving
			Change PR146 to 500 ohm	QDP Tuner
16	2011/10/12	P49/P49/P50	Change +1.2ALMP/+VRAM_1.SVSP/+VGA_CORE input to +12V2	For layout easily
		P51	Update PU13 (IR3565) part number	New part number released
17	2011/10/12	P51	Update PU16 to 499 ohm	old part x code
18	2011/10/14	P44/P46/P48/P49	Remove PC46/PC68 Change PC22/ PC23/PC27/PC79/PC82 bom structure to "a" Change PC21/PC24/PC48/PC59/PC81 PW to SE00000QK00	For C18 request
19	2011/10/14	P43	add PC46/PC55/PC68	For EHD request
			add PR9/PR47/PR92/PR181	For C18 request
20	2011/10/14	P51	Change PC122 PW to SE026474E80	For DUE request
21	2011/10/17	P52	add PR182/PR183/PR184/PR185/PR186/PR187	For EMI request
22	2011/10/18	P52	change PR182/PR183/PR184/PR185/PR186/PR187 to 0805 size	For C18 request
23	2011/10/18	P52	Midify PU14,15,PU16,17 Enable Signal	Modify enable signal error
24	2011/10/25	P44	Remove PR26 in BOM	Modify PSU_DG signal
25	2011/11/09	P46	Change PR9 net name from +V_5V to +5VSB	
		P47	Change PC58 net name from +V_5V to +5VSB	
		P47	Change PC58 net name from +V_3.3V to +3VSB	Design change
		P51	add BOM Structure "a" at PR105 and PR106	
26	2011/11/14	P51	change PR105 and PR106 to 0805 size	
		P53	remove PQ0CAP PC184 and PC212 add BOM structure "100W" to PC177 add BOM structure "a" to PC181 and remove "a" from PC183 add PC244, PC245, PC246, PC247 add PC242, PC243, PC212, PC241, PC248, PC249 with BOM Structure"a" add BOM structure "a" to PC208	Design change
			add BOM structure "D18a" to PR88, PR90, PR93, PC221-PC260	BOM control
27	2011/11/16	P50	change PW from SB000009610 to SB000009Q80 of PQ1,PQ15,PQ16	Material shortage
28	2011/11/17	P43, P48	change PR from SB000009610 to SB000009Q80 of PQ1,PQ15,PQ16	Material shortage
29	2011/11/18	P55	change PR93 to 27K, and PR88 to 20K	Design change
30	2011/11/18	P48	change PR47.2 net name from "+V_5V" to "+5VSB"	Design change
31	2011/11/23	P48	Add BOM Structure "100W" in PR116, PR117, PR118, PR122 and PC113	cost down
		P51	Add PR188 with BOM structure "65W"	
32	2011/11/24	P52	Add PR189 with BOM structure "a"	Design change
33	2011/11/28	P50	change PR88 to 10K and PR93 to 40.2K	
		P53	remove BOM Structure"a" of PC248	Design change
34	2011/11/29	P50	change PR107, PR112, PR116, PR124, PR128, PR133---1.58K change PR109, PR114, PR118, PR126, PR130, PR137---1.27K change PC119, PC110, PC113, PC115, PC117, PC119---0.470(K7R) PR141---2.05K PR135---1.78K PR145---1.82K	Design change
		P48, P49	change PR57, PR71 to 2R2	
35	2011/12/01	P51	add PR191-4.7K add PR150-49.9-ohm add PQ5 add PR188	
36	2011/12/7	P50	Change PR86, PR88, PR90, PR93 resistor value	Change VGA_CORE VID
		P43	remove BOM Structure"a" of PC46	For EMI request
37	2011/12/13	P51	Add PU13 BOM Structure "65W" for SA00005J200 Add PU13 BOM Structure "100W" for SA00005BP00	Part Number divided
38	2012/1/31	P43	PU2 change to SA00008000 (E78033)	Design change
		P50	PR139, PR145 change to 1.96K	Loadline finetune
		P47	PC59=0.10P , PR48=160K , PR50=270K	Design change
39	2012/2/1	P43	PU2 change to SA00004CY10 (RT9061) Add PU1	Design change

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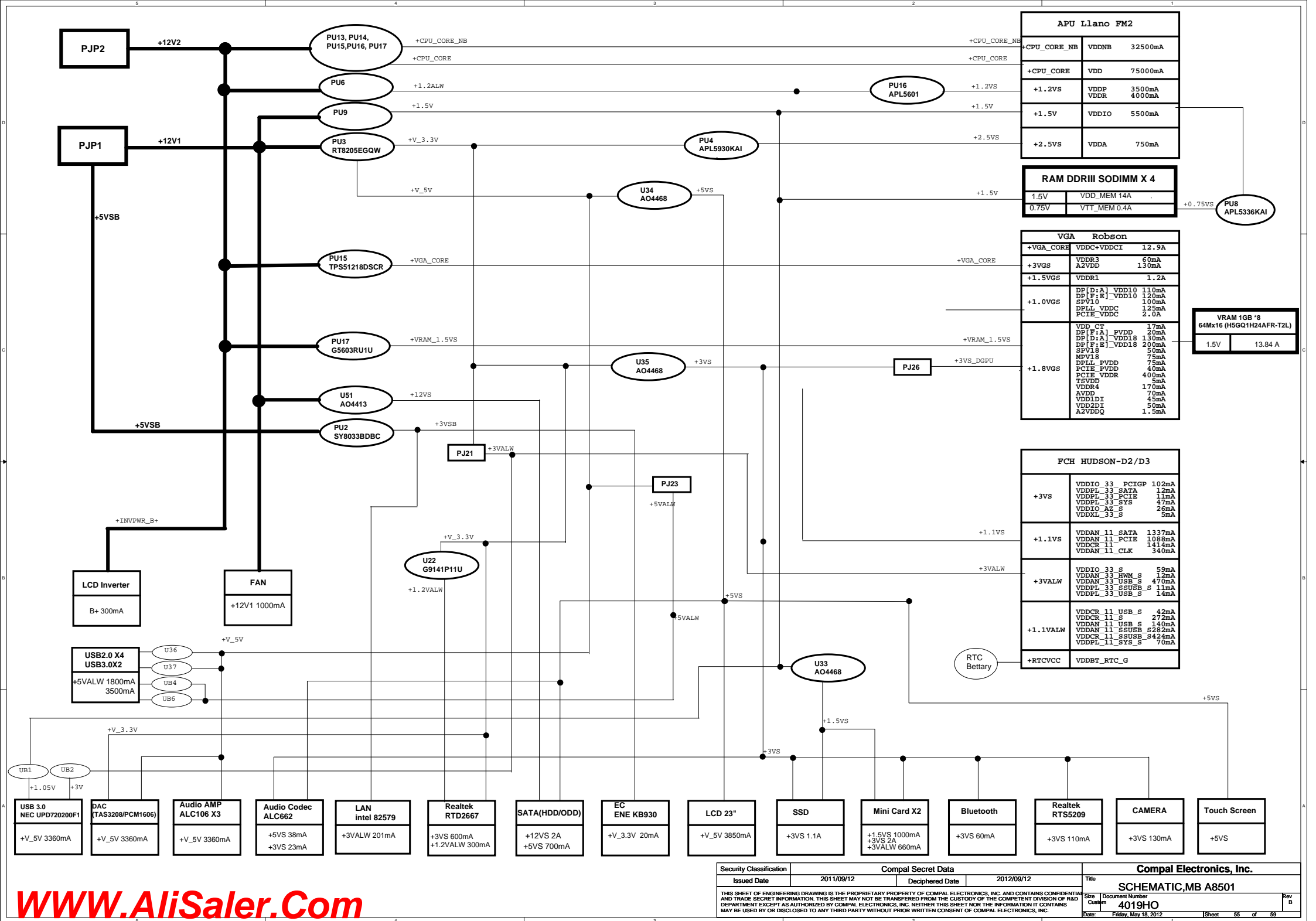
2017/06/12

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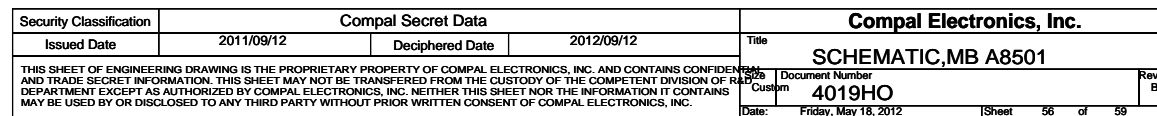
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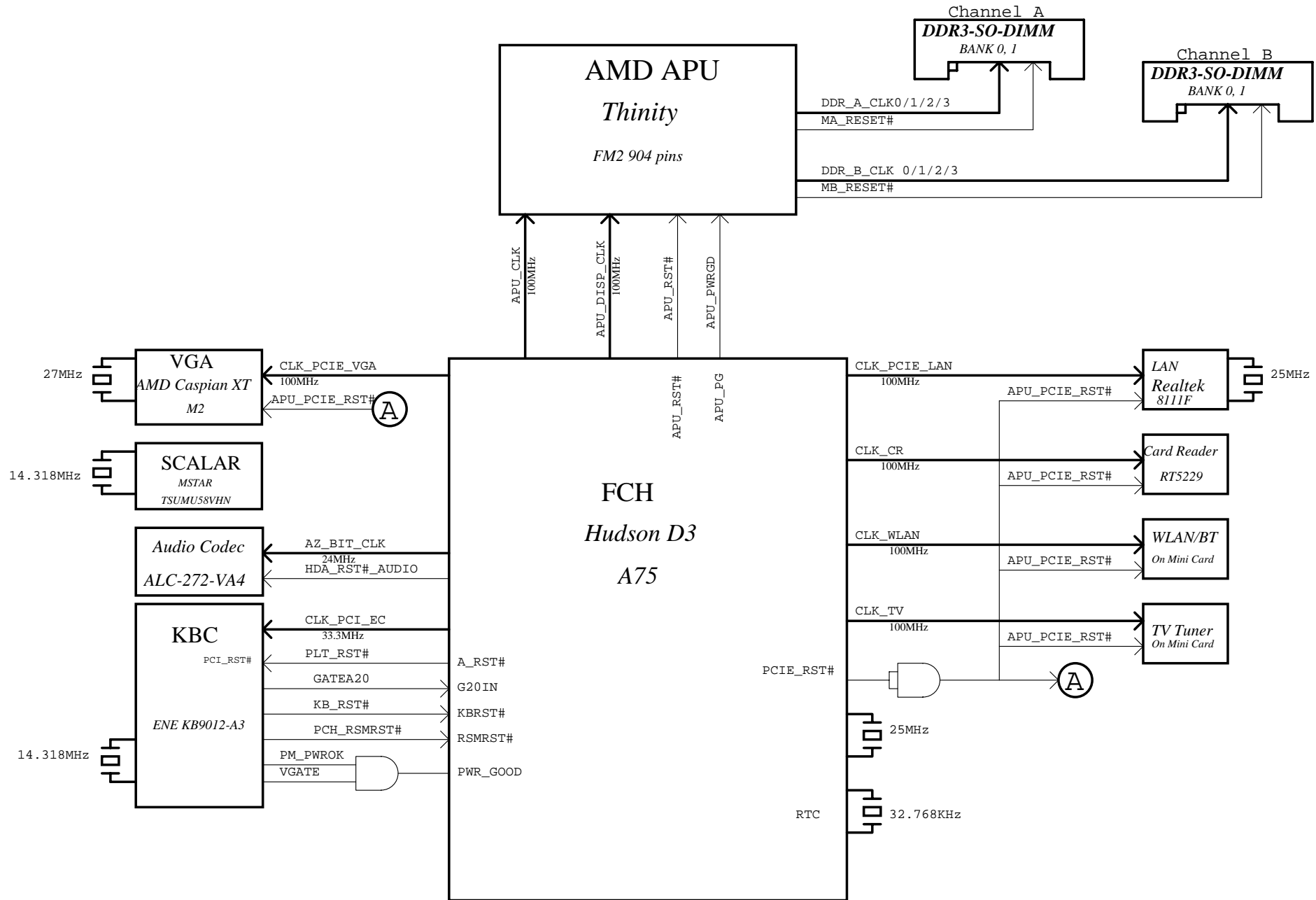
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MODEL NAME: QLA13 Power Sequence Block Diagram (Discrete)
PCB NAME: LA8501P
REVISION: 0.1
DATE: 2010/10/26



Clock and Reset Diagram



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HW schematic change list

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1	01/20	P15	R1764 change to 1M	BOM ERROR
2	01/20	P18	R1737,R1738 BOM change to @	BOM ERROR
3	01/20	P29	Add R1803	For HDMI Votage
4	01/20	P40	C612 change to 0805	For DFX
5	01/20	P40	JBT1 change to 8 pin ACES_87212-08G0L	For ASSY to move location
6	01/20	P31	Remove R525,C681 & R524,C681	For EMI
7	01/28	P42	H2,H4 change to 4P0	For ME
8	01/28	P42	Add 10u C1908,C1909 for +V_5V	For ESD
9	01/28	P39	Add 1u C1906,C1907 for +V_3.3V&+USB_VCCA	For ESD
10	01/28	P29	Add C1910,C1911 for +V_3.3V	For HDMI IN Re-driver
11	01/28	P29	Remove ESD DIODE D12,D13,D16,D18	For HDMI IN Re-driver
12	01/29	P05	Remove HDT1	For ESD
13	01/29	P31	Remove Q102,Q120	For EMI
14	02/01	P41 P39 P29 P37 P40 P16	Add C1916 0.1u on SENSE_BD +3VSB Add C1914 0.1u on S3USB_ON Add C1912 0.1u on IO Conn. +3VALW Add C1913 0.1u on MUTE_CODEC Add C1915 0.1u on BT_RESET Change C247 2.2u to 10u	For ESD
16	02/24	P33 P39 P40	Add RC on external& internal USB D-	AMD Errata 40
17	03/16	P37	Add PWR_65W#100W GPIO	
18	03/19	P28	Add PANEL_C_2	
19	04/16	P41	Del SW1	
20	05/04	P29	Add D10/D11 for ESD	
21				
22				
23				

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